HIGH PERFORMANCE COMPUTER ARCHITECTURE 19-11-2024

MATRICULATION NO.__________________

SURNAME____________________

FIRST NAME____________________

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Consider a bus-based multicore that supports a cache-coherence protocol called MOSI. Compared to the well-known MESI protocol, the MOSI protocol uses a state called O (Owned) and does not have the E state. A copy in O state is like a SM copy in Dragon: the owned copy is modified and the "owner cache" has the responsibility to provide the copy once a BusRd transaction involves that copy; at the same time, the M state is now simplified, as it doesn't have to update memory on Flush (only Flush* transactions appear in this protocol). A copy enters the O state if another cache needs a copy (for reading) while that copy is in M state; on a local read, local write or other bus transactions, the O copy behaves like an S copy.

1a) [Points 8/30] Draw the diagram of the MOSI protocol according to the above description.

1b) [Points 22/30] Assuming a cost of 1cc (1 clock-cycle) for read/write operations, 90cc for BusRd or BusRdx transactions, 60cc for BusUpgr, 20 cc for Flush* and 30cc for Flush. Evaluate the total cost (in clock-cycles) for the following streams:

	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
stream-1 MOSI	PrRd1						
	PrWr1						
	PrRd1						
	PrWr1						
	PrRd2						
	PrWr2						
	PrRd2						
	PrWr2						
	PrRd3						
	PrWr3						
	PrRd3						
	PrWr3						
	TOTAL						

	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
stream-2 MOSI	PrRd1						
	PrRd2						
	PrRd3						
	PrWr1						
	PrWr2						
	PrWr3						
	PrRd1						
	PrRd2						
	PrRd3						
	PrWr3						
	PrWr1						
	TOTAL						

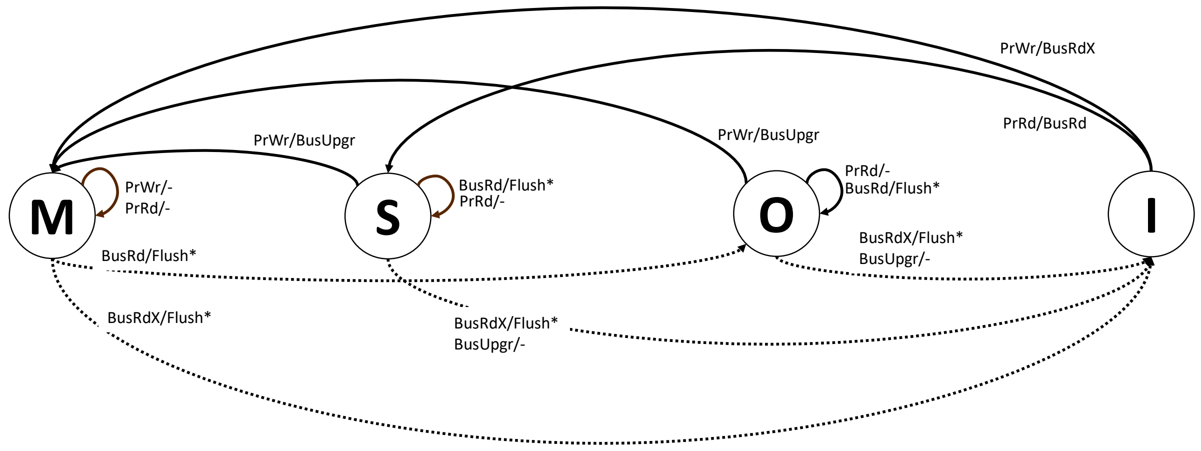
	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
stream-3 MOSI	PrRd1						
	PrRd2						
	PrRd3						
	PrRd3						
	PrWr1						
	PrWr1						
	PrWr1						
	PrWr1						
	PrWr2						
	PrWr3						
	TOTAL						

EXERCIZE 1a)

M-state: PrRd and PrWr are exactly as in MESI; however, when there is a BusRd, the copy enters into O-state while providing the copy to the requesting cache (via a Flush* transactions) without the need of updating the memory; since it is now the cache with the copy in O-state that has the responsibility to provide a shared-modified copy, the memory is updated on replacement (i.e., for cache conflicts) of M copies or O copies. If a BusRdX transaction is observed in M-state, that cache provides the copy (via a Flush* transaction) to the requesting cache and change its state from M to I.

O-state: since it is now this state that has the responsibility to update memory on replacement or to provide the copy to other caches, the local read or write behave like in the S-state; similar for BusRd, BusRdX or BusUpgr the O-state will have the same behavior for operations and transactions happening in the S-state.

S-state: since there is no E-state, when there is a read-miss, the copy enters in S-state; in S-state, a PrRd doesn't change the state, while a PrWr brings the copy in M-state, while invalidating all the other copy with a BusUpgr; on a BusRdX, the copy is provided to the other caches via a Flush* transaction and set to I in the local cache; on a BusUpgr the copy is invialidated locally.



EXERCIZE 1b)

	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
stream-1 MOSI	PrRd1	S	I	I	BusRd	Mem.	90
	PrWr1	M			BusUpgr		60
	PrRd1	M			-		1
	PrWr1	M			-		1
	PrRd2	O	S		BusRd/Flush*	C1	90+20
	PrWr2	I	M		BusUpgr		60
	PrRd2		M		-		1
	PrWr2		M		-		1
	PrRd3		O	S	BusRd/Flush*	C2	90+20
	PrWr3		I	M	BusUpgr		60
	PrRd3			M	-		1
	PrWr3			M	-		1
	TOTAL						496

	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
stream-2 MOSI	PrRd1	S	I	I	BusRd	Mem.	90
	PrRd2	S	S		BusRd/Flush*	C1	90+20
	PrRd3	S	S	S	BusRd/Flush*	C1/C2	90+20
	PrWr1	M	I	I	BusUpgr		60
	PrWr2	I	M		BusRd/Flush*	C1	90+20
	PrWr3		I	M	BusRd/Flush*	C2	90+20
	PrRd1	S		O	BusRd/Flush*	C3	90+20
	PrRd2	S	S	O	BusRd/Flush*	C3	90+20
	PrRd3	S	S	O	-		1
	PrWr3	I	I	M	BusUpgr		60
	PrWr1	M		I	BusRd/Flush*	C3	90+20
	TOTAL						981

	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
stream-3 MOSI	PrRd1	S	I	I	BusRd	Mem/	90
	PrRd2	S	S		BusRd/Flush*	C1	90+20
	PrRd3	S	S	S	BusRd/Flush*	C1/C2	90+20
	PrRd3	S	S	S	-		1
	PrWr1	M	I	I	BusUpgr		60
	PrWr1	M			-		1
	PrWr1	M			-		1
	PrWr1	M			-		1
	PrWr2	I	M		BusRd/Flush*	C1	90+20
	PrWr3		I	M	BusRd/Flush*	C2	90+20
	TOTAL						594