HIGH PERFORMANCE COMPUTER ARCHITECTURE 23-11-2022 MATRICULATION NO._____

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SURNAME_____

FIRST NAME_____

1) (POINTS 8/30) Consider a bus-based multicore that supports a new cache-coherence protocol called MESIF. Compared to the well-known MESI protocol, the MESIF protocol adds a 5th state called F (Forward). A copy in F state is like an S copy but the cache which holds it has the responsibility to provide (forward) the copy once a BusRd transaction involves that copy; at the same time, the S state is now simplified, as it doesn't have to respond to cache-to-cache transfers (Flush* transactions) due to a BusRd. There will be at most one cache holding a copy in the F state; on a PrRd miss, if the are other shared copies, the state will be F, whilst if another F copy observes the BusRd will go to S. Both F and S states are clean shared states. If the copy in F state is eventually evicted, there will be no copy in the F state: in this case the copy will be provided by the memory.
1a [Points 8/30] Draw the diagram of the MESIF protocol according to the above description.

M E S F I

1b) [Points 22/30] Assuming a cost of 1cc (1 clock-cycle) for read/write operations, 90cc for BusRd or BusRdx transactions, 60cc for BusUpgr, 20 cc for Flush* and 30cc for Flush. Evaluate the total cost (in clock-cycles) for the following streams:

stream-1 MESIF

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1						
PrWr1						
PrRd1						
PrWr1						
PrRd2						
PrWr2						
PrRd2						
PrWr2						
PrRd3						
PrWr3						
PrRd3						
PrWr3						
TOTAL						

stream-2 MESIF

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1						
PrRd2						
PrRd3						
PrWr1						
PrWr2						
PrWr3						
PrRd1						
PrRd2						
PrRd3						
PrWr3						
PrWr1						
TOTAL						

stream-3

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1						
PrRd2						
PrRd3						
PrRd3						
PrWr1						
PrWr1						
PrWr1						
PrWr1						
PrWr2						
PrWr3						
TOTAL						