HIGH PERFORMANCE COMPUTER ARCHITECTURE 23-11-2022 MATRICULATION NO._____

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SURNAME_____

FIRST NAME_____

1) (POINTS 8/30) Consider a bus-based multicore that supports a new cache-coherence protocol called MESIF. Compared to the well-known MESI protocol, the MESIF protocol adds a 5th state called F (Forward). A copy in F state is like an S copy but the cache which holds it has the responsibility to provide (forward) the copy once a BusRd transaction involves that copy; at the same time, the S state is now simplified, as it doesn't have to respond to cache-to-cache transfers (Flush* transactions) due to a BusRd. There will be at most one cache holding a copy in the F state; on a PrRd miss, if the are other shared copies, the state will be F, whilst if another F copy observes the BusRd will go to S. Both F and S states are clean shared states. If the copy in F state is eventually evicted, there will be no copy in the F state: in this case the copy will be provided by the memory.
1a [Points 8/30] Draw the diagram of the MESIF protocol according to the above description.

M E S F I

1b) [Points 22/30] Assuming a cost of 1cc (1 clock-cycle) for read/write operations, 90cc for BusRd or BusRdx transactions, 60cc for BusUpgr, 20 cc for Flush* and 30cc for Flush. Evaluate the total cost (in clock-cycles) for the following streams:

stream-1 MESIF

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1						
PrWr1						
PrRd1						
PrWr1						
PrRd2						
PrWr2						
PrRd2						
PrWr2						
PrRd3						
PrWr3						
PrRd3						
PrWr3						
TOTAL						

stream-2 MESIF

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1						
PrRd2						
PrRd3						
PrWr1						
PrWr2						
PrWr3						
PrRd1						
PrRd2						
PrRd3						
PrWr3						
PrWr1						
TOTAL						

stream-3 MESIF

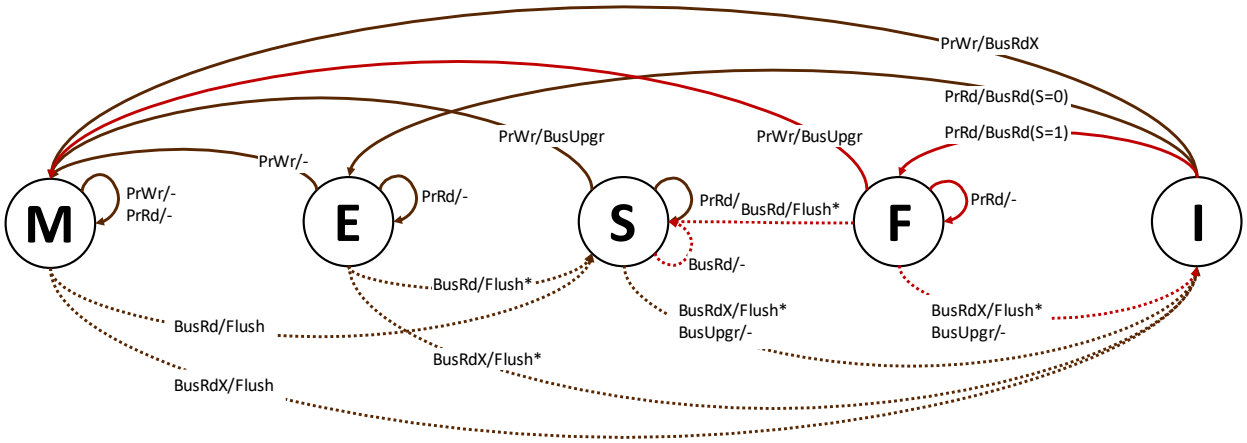
Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1						
PrRd2						
PrRd3						
PrRd3						
PrWr1						
PrWr1						
PrWr1						
PrWr1						
PrWr2						
PrWr3						
TOTAL						

EXERCIZE 1a)

First, we start drawing the states of the MESI protocol (except for S state – see brown lines), then let's focus on S and F states.

S-state: PrRd and PrWr are exactly as in MESI; also, BusRdX and BusUpgr, as in MESI, cause an invalidation of the local copy; BusRdX will also provide a copy (useful, e.g., in the case of write-miss (PrWr from I)) to be written partially;
differently from MESI, now a BusRd - snooped from a cache with a copy in S-state – will NOT be followed by a Flush*: the cache with the shared copy in F-state will provide such copy, eventually – if such copy has been evicted in the meantime, the memory will intervene.

F: state: PrRd and PrWr are exactly like for the S-state (remember that F is a shared clean state); like in S-state, the BusRdX and BusUpgr transaction cause a local invalidation, with the Flush* following the BusRdX; we enter the F-state on a read-miss once the shared-line indicates that there exist other copies in the system (S=1), so the newly acquired copy is shared; when a BusRd is snooped, this cache has the responsibility to provide the copy via a Flush* and its state will be then demoted to S (its duty is finished, the other cache with the shared copy will get the new copy in F state – it is the only possibility for a BusRd – the other is with S=0, which is not this case).



EXERCIZE 1b)

stream-1 MESIF

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1	E	I	I	BusRd(S=0)	Mem	90
PrWr1	M			-	-	1
PrRd1	M			-	-	1
PrWr1	M			-	-	1
PrRd2	S	F		BusRd(S=1),Flush	C1	90+30
PrWr2	I	M		BusUpgr	-	60
PrRd2		M		-	-	1
PrWr2		M		-	-	1
PrRd3		S	F	BusRd(S=1),Flush	C2	90+30
PrWr3			M	BusUpgr	-	60
PrRd3			M	-	-	1
PrWr3			M	-	-	1
					TOTAL	457

stream-2 MESIF

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1	E	I	I	BusRd(S=0)	Mem	90
PrRd2	S	F		BusRd(S=1),Flush*	C1	90+20
PrRd3	S	S	F	BusRd(S=1),Flush*	C2	90+20
PrWr1	M	I	I	BusUpgr	-	60
PrWr2	I	M		BusRdX,Flush	C1	90+30
PrWr3		I	M	BusRdX,Flush	C2	90+30
PrRd1	F		S	BusRd(S=1),Flush	C3	90+30
PrRd2	S	F	S	BusRd(S=1),Flush*	C1	90+20
PrRd3	S	F	S	-	-	1
PrWr3	I	I	M	BusUpgr	-	60
PrWr1	M		I	BusRdX,Flush	C3	90+30
					TOTAL	1021

stream-3 MESIF

Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
PrRd1	E	I	I	BusRd(S=0)	Mem	90
PrRd2	S	F		BusRd(S=1),Flush*	C1	90+20
PrRd3	S	S	F	BusRd(S=1),Flush*	C2	90+20
PrRd3	S	S	F	-	-	1
PrWr1	M	I	I	BusUpgr	-	60
PrWr1	M			-	-	1
PrWr1	M			-	-	1
PrWr1	M			-	-	1
PrWr2	I	M		BusRdX,Flush	C1	90+30
PrWr3		I	M	BusRdX,Flush	C2	90+30
					TOTAL	614