

Roberto Giorgi

Curriculum Vitæ (2 October 2026)

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Main Facts

- Roberto Giorgi is an Associate Professor at Dept. of Information Engineering, University of Siena, Italy.
- He has received the eligibility (Italian National Abilitation) as Full-Professor since 30th March 2018.
- For one year, he was Research Associate at the University of Alabama in Huntsville, USA.
- He received his PhD in Computer Engineering and his MS in Electronics Engineering, Summa cum Laude both from University of Pisa, Italy.
- He coordinated the European Project AXIOM (3.9Meuro cost, 2015-2018, 7 partners), about designing and manufacturing the next generation board for Cyber-Physical Systems.
- He coordinated the TERAFLUX project (8.5Meuro cost, 2010-2014, 11 partners) in the area of Future and Emerging Technologies for Teradevice Computing.
- He is member of the HiPEAC Network of Excellence (High Performance Embedded-system Architecture and Compilation) since 2004.
- He was Deputy Steering Committee in the HiPEAC, Application leader in the ERA project (Embedded Reconfigurable Architectures), participated to SARC (Scalable ARChitectures) and attracted more than 3 Million Euro of Research Funding to the University of Siena in the last decade.
- He took part in ChARM project, developing software for performance evaluation of ARM-processor based embedded systems with cache memory for VLSI Inc..
- He has been IEEE Judge for the IEEE-CSIDC (Computer Society International Design Competition).
- He led the project "Bluesign Translator", which received a 5th worldwide prize by IEEE and top companies, and received the FORUM-P.A. prize by the Italian Ministry of Technological and Scientific Innovation, as absolute winner in the category of "actions for the social integration of disadvantaged people through ICT".
- He has been selected by the European Commission as an independent expert for evaluating several ICT and HPC European Projects.
- He is co-author of more than 160 scientific papers.
- He is Ministry-appointed deputy and director for Uni.Siena in the National Consortium for Informatics (CINI).
- His current interests include Computer Architecture themes such as Embedded Systems, Multiprocessors, Memory System Performance, Workload Characterization, Reconfigurable Computing, High-Performance Computing.
- He is a Lifetime Member of ACM, a Senior Member of IEEE and a Distinguished Contributor of the IEEE Computer Society.

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1 Appointments

Visiting Professor Feb.-Sept. 2025
Barcelona Supercomputing Center, Spain

- "Barcelona Zettascale Laboratory - Hardware Design for High-Peroformance RISC-V"

Associate Professor of Computer Architecture (with tenure) Oct. 2006-present
University of Siena, Dept. of Information Engineering, Siena, Italy

Assistant Professor of Computer Architecture (with tenure) Mar. 1999-Sept. 2006
University of Siena, Dept. of Information Engineering, Siena, Italy

Post-Doctoral Researcher Feb. 1999-Jan. 2000
The University of Alabama in Huntsville, AL, USA

- "Experimental Research for the Evaluation of Multithreaded Architectures" (**NSF** grant #9805216)
- "Multithreading Systems" (Italian National Research Council (**CNR**) grant #203.15.9)

Visiting Scholar May 1998
University of Belgrade, Serbia, Yugoslavia
Visiting Scholar Jul. 1997-Aug.1997
University of Texas in Arlington, TX, USA
Visiting Scholar Jul. 1996-Aug.1996
University of Washington, WA, USA

2 Education

PhD in "Information Engineering: Electronics, Informatics, Telecom." Oct. 1995-Sept. 1998
University of Pisa, Pisa, Italy
"Evaluation of a Coherence Protocol for Eliminating Passive Sharing in Shared-Bus Multithreaded Multiprocessors"
Thesis advisor: Prof. Cosimo Antonio Prete

MEng in "Electronics Engineering" July 1995
University of Pisa, Pisa, Italy
"Performance Evaluation of Multiprocessor Systems, based on Real Traces Analysis"
Thesis advisor: Prof. Cosimo Antonio Prete
Mark: **Summa cum Laude** (**110/110+Laude**)

High-School Diploma "Scientific Lyceum" July 1983
Viareggio LU, Italy
Mark: **60/60**

3 Awards

- 2024(Dec) Technology Transfer Award 2024 by HiPEAC (High-Perforamnce Edge And Cloud computing EU Network of Excellence) for the Bluesign project for encoding Sign Language for the Deaf.
- 2022 (Jun) Best Keynote Speaker award at IEEE MECO/CPSIoT 2022 conference (selected among Luca Benini and Letizia Iaccheri).
- 2017 (Jun) ACM Recognition of Service Award for chairing the ACM Computing Frontiers 2017 conference.
- 2014 (Jun) Outstanding Contribution Award at IEEE MECO 2014 conference.
- Best paper awards for works [C74], [C60], [C42], [C2] (see below).
- 2006 (May) FORUM P.A./CNIPA Award by **Italian Ministry of Innovation and Technologies** for the best action to accessibility of public administration by the disable through the project "BlueSign Translator" (**absolute winner in the category**). Web sites: http://www.bluesign.it/ e https://it.wikipedia.org/wiki/Blue_Sign.
- 2002 (Jun) IEEE Award (5th worldwide price 2000 USD) for the realization of a "Sign Language Translator" based on Bluetooth Technology for helping the Deaf in a course projects, IEEE Computer Science International Design Competition (CSIDC).

4 Technology Transfer

- 2023-25 Public-Private Partnership: setup and steering contribution to the formation of a partnership between Univ. of Siena and a private consortium (related to a 1 PFLOPS HPC infrastructure in Siena).
- 2021-22 Cooperation Agreement with Quest-IT (a company working in the Artificial Intelligence area) on technology transfer regarding UNISI proprietary technologies.
- 2014-2017 Coordinating the EU-funded Research and Innovation Action AXIOM, which realized through partner SECO an FPGA-based Italian-manufactured single computer board.
- 2007-2009 Cooperation Agreement with RAI (RADIOTELEVISIONE ITALIANA) for the implementation of advanced solutions for the integration of automatic translation systems of Sign Language for the Deaf in the television.
- 2003-2008 Cooperation with Italian Association for the Education of the Deaf (AIES, Associazione Italiana Educazione Sordi) to support the study of a multimedial system for communicating in Italian Sign Language (LIS, Lingua Italiana dei Segni).
- 1998(Nov)-1999(Jan) Contract for "Performance Evaluation of Coherence Protocols for Single-Chip Embedded Multiprocessors" at the Department of Information Engineering, University of Pisa.
- 1995(Sep)-1995(Dec) Contract for "Performance Evaluation of Multiprocessor System under Different Software Workload" at the Department of Information Engineering, University of Pisa.
- 1995(Sep)-1995(Oct) Cooperation with VLSI Tech. Inc., San Jose, CA, U.S.A. to support the realization of X/MOTIF Graphical Interface for the commercial software "ChARM - JumpStart 3.0".

5 Fields of Interest and Impact

- **According to SCOPUS, my FWCI is 2.14 (June 2024)** - The Field-Weighted Citation Impact is the ratio of citations received relative to the expected world average for the subject field, publication type, and publication year.
- **Scalable, Adaptive and Reconfigurable Systems - enhancing High-Performance Computing architectures** Current High-Performance systems (ranging from the Cloud-Computing to the Embedded-HPC) need more localization of the resources, and the paradigms of Edge-Computing and Fog-Computing have been proposed to provide a form of proxy to several cloud-based services. At the same time, we are entering the Cyber-Physical age, in which both objects and people will become nodes of the same digital network for exchanging information. Therefore, in our imagination, the general expectation is that "things" or systems will become somewhat smart as people, allowing rapid and close interactions not only system-system but also human-system, system-human. More scientifically, we expect that such systems will at least react in real-time, have enough computational power for the assigned tasks, consume the least possible energy for such task (energy efficiency), scale up through modularity, allow for an easy programmability across performance scaling and exploit at best existing standards at minimal costs. The whole set of these expectations imposes scientific and technological challenges that must be properly addressed. In this line of research (projects AXIOM and ERA), we aim to research new software/hardware architectures to meet the above expectations. The technical approach aims at solving fundamental problems to enable easy programmability of multi-core multi-board systems through the open-source OmpSs programming model, leveraging Distributed Shared Memory (DSM) inspired concepts across the modules. The OmpSs will allow accelerating functions through an FPGA (Agility). In particular, to the best of our knowledge, this is the first time that DSM will be effectively demonstrated on an embedded modular system (eXtensibility). Modular scalability will be possible thanks to a fast interconnect that will enrich the module. To this aim, innovative modular RISC-V or ARM-based boards with enhanced capabilities for interfacing with the physical world have been designed and demonstrated in key scenarios such as Smart video surveillance, Smart Living/Home (Domotic) or other [J35], [J33], [J32], [J30], [J29], [J28], [J27], [J25], [J24], [B10], [C77], [C75], [C69], [C68], [C67], [C66], [C65],[C64],[C63],[C62],[C61],[C60],[C56],[C54],[C53],[C47],[C46],[C38],[C41],[C24]. **Impact: Foundational aspects of innovative computer architectures are enabling more and more applications.**
- **Architectures and Tools for Many-Core systems - towards Big-Data systems** The ever increasing pace of data poses challenges at several levels in the software-hardware architectures. In this line, future Teradevice Systems, i.e. systems with more then a trillion (10^{12}) transistors in a single package or multi-layer chip, exhibit a large amount of parallelism (e.g., general purpose 1000 cores) has been explored (such systems have been a practical reality since 2018 with wafer-scale chips and related commercial products). Current applications and programming models are not yet using this type of systems efficiently. The work done in this field of research regards the development of architectures that both build on existing solutions at the architectural level and try to enable the execution of parallel programs even in the case of sequential programming models. This is made possible by exploiting a parallel generation and scheduling of threads and combining concepts of dataflow. Big-data can be managed in a very efficient way using Dataflow Supercomputing [G6], which can rely on Dataflow Engines now available on

the market [B3]. An essential aspect becomes to be able to assess the performance of these new platforms that not yet exist, using appropriate tools [J32], [J31], [J22], [J21], [J20], [J18], [J17], [J13], [B10], [C76], [C59], [C58], [C57], [C55], [C50], [C45], [C49], [C48], [C42]. In addition, applications are becoming more complex, requiring more computational resources as they need to process larger and larger amounts of data ("big-data"); a typical example is bioinformatics applications as we need a shorter time to analyze biological data and have precise information on the health status of a patient. Processing may not necessarily be a classic data-parallel problem: in the general case of irregular applications, the effort required by the programmer can be very high or even not feasible. For this reason, in this line of research, we examine the methodologies that enable a more efficient execution, regardless of what the programmer specifies, by improving the hardware/software interface. The contribution in this area is a proposal for a radical change in the way applications run on the architecture, using however minimal changes to the architecture itself. The proposal is currently focusing on the use of an extended instruction set ("called T-Star", consisting of only six instructions) and its architectural support. In order to demonstrate the applicability to current computing systems we used the x86_64 architecture, but we analyzed the feasibility of other previous architectures, such as the Cell Processor and more recently on FPGA architectures [J35], [C36],[C35],[C34],[C33],[C31]. **Impact: the data economy and data deluge demand support for more efficient hardware architectures which are key for the many grand-challanges and everyday life.**

- **Low-Power techniques for Embedded Systems** One of the most critical parts of an embedded system is the cache memory since it affects performance and large portions of the power consumption. In particular, the losses (leakage) continue to be a problem despite the use of new materials with a high dielectric constant (Hi-K) even in the 11nm technology nodes and at normal operating temperatures (over 30 degrees Celsius). An innovative proposal is based on the filtering effects of a non-low-power cache stage followed by a low-power cache stage. Significant improvements can be achieved at virtually negligible costs in terms of area and complexity [C37],[C32],[C30],[C29]. **Impact: low-power research provides benefits at any level of computing.**

- **Design techniques for architectural support of Elliptic Curve Cryptography** The cryptographic systems based on elliptic curves (or ECC Elliptic Curve Cryptography) have the advantage of working with operands of a length of at least one order of magnitude lower than that of cryptographic standards now commonly in use, such as RSA, DSA, Diffie-Hellman, El-Gamal. Because of this important feature, cryptosystems based on elliptic curves are particularly suitable for use on smart cards and devices like mobile and embedded applications. Typically, there are two possible solutions to improve the performance of ECC systems: the first is the optimization of the software, the second is the realization of hardware arithmetic coprocessors. The software implementation is certainly flexible, but the performance that would be obtained in the embedded devices is inadequate; on the contrary, hardware processing is expensive and does not offer the desired flexibility. The research carried out, using the instruction set of ARM processors, widely used in embedded applications, shows promising results. The architectural support that involves on the one hand the minimum hardware changes has been identifiedi, in particular the importance of a carry-less multiplication for speeding up the computation on the Galois Field. This has also other benefits in terms of reducing the execution time and the overall used resources [J16],[J14],[J9],[C22],[C20]. **Impact: after these papers, x86_64 commercial products are including the carry-less multiplication instruction (CLMUL) in their instruction set.**

- **Evaluation and proposal of a new microprocessor architecture based on multithreading and dataflow concepts, which enables to overcome traditional limitations of Superscalars and VLIWs** In this research line, it has been analyzed the possibility of using a new processor architecture that could considerably improve the performance of current architectures based mainly on the Superscalar and VLIW paradigms. This research has led to the definition of a new type of microprocessor that builds on the concepts of dataflow and expresses them fully in current multithreaded systems. The architecture is called Scheduled Data-Flow (SDF) and it has been expanded into novel models called Decoupled Threaded Architecture (DTA). Later developments led to the TERAFLUX architecture. Several generations of simulators have been developed in order to arrive lately to the model of a full-system 'as-is' running an off-the-shelf Linux Operating System and consisting of multiple cores (up to 32 per node have been explored) and multiple nodes. The results were very encouraging already with the first simulated prototypes and demonstrate that this type of architecture allows not only to achieve superior performance with respect to current superscalar processors and VLIWs but also to fully exploit the thread-level parallelism, thus overcoming the limitations of scalability of the processor internal resources (e.g., limited instruction level parallelism) of current architectures [J29], [J26], [J22], [J21], [G6], [B9], [B8], [B7], [B6],[B5],[B4],[B3],[J19],[J17],[J8],[J7],[J6],[J5],[C59],[C51],[C44],[C43],[C40],[C39],[C28],[C17],[C12]. **Impact: dataflow principles continue to indicate the most efficient way to perform computing - more development are expected in the near future; dataflow computation is also behind the recent wafer-scale systems.**

- **Innovative solutions for cache-coherence of single-chip multiprocessor systems under thread migration** In this line of research, a new coherence protocol called PSCR (Shared Passive Copy Removal) was proposed and evaluated in the case of shared-bus, shared-memory multicores. This architecture is particularly attractive given its low cost and simplicity, and in fact, it has been adopted since the year 2000 by all major processor manufacturers. While it is necessary to introduce private cache memories to overcome the limitations of excessive traffic on the shared bus, we must also introduce mechanisms to manage the consistency of multiple copies of the application

data. This problem is exacerbated by thread migration to available cores, in turn, necessary to balance the load in the machine. However, this research highlighted that a considerable part of the traffic is unnecessary because it is due to copies that mistakenly appear as shared while they are actually private: this situation has been called "passive sharing". The proposed solution consists of a novel coherence protocol (PSCR) that completely eliminates passive sharing. The evaluation of such protocol demonstrated that PSCR can achieve a higher scalability than six other protocols known in the literature or widely used, such as the MESI protocol. The results showed that with the use of PSCR, multicores with more than 30 cores are feasible even with a simple and inexpensive solution such as the shared-bus interconnect [J3],[J2],[J1],[C10],[C7],[C4],[C3],[C2],[C1]. **Impact: at least 16 patents have been citing this work; this study was carried out at the end of 20th century, nowadays 32-core systems have become a common reality.**

- **Study of solutions for improving performance of Web-Servers and Data-Base Management Systems (DBMS)** Web servers and DBMSs (Database Management Systems) are particularly critical from the point of view of performance. E.g., E-Commerce systems, OLTP systems (Online Transaction Processing) and DSSs (Decision Support Systems) are implemented with an N-tier distributed architecture or also simply with a three-tier architecture, in which the second layer acts primarily as a web server and the third layer acts primarily as a DBMS (being the first layer consists of the client or Web browser). To cope with a high number of requests, the typical solution is to use a Network of Workstations (or Clusters). In cases where the single node constitutes a multicore system, it is necessary to use every possible solution to maximize performance. In particular, taking into account the organization of the system, the machine load (workload) consists of intense multitasking activity (generated by both Web client requests and DB queries) that involves a strong commitment to the Operating System (e.g., Scheduler, Virtual Memory) to obtain a balanced load. Taking this platform as a case study, we tried to highlight possible architectural solutions to significantly improve the machine's performance. Through the combined intervention on restructuring kernel data, operating system virtual mapping, OS scheduler and the coherence protocol, we found that it is possible even to double the performance of a multicore system. The evaluation methodology is based on well-known benchmarks such as TPC-W and TPC-D [J12],[J11],[J10],[C21],[C19],[C16],[C15],[C14],[C13],[C11],[C9]. **Impact: most of the internet architecture is based in the three-tier model - optimizing the workloads leads to sustenaibilty and greener availability.**

- **Handheld Multimedia Devices for the Deaf** Starting from the analysis of the actual needs of the Deaf, it emerged that the Deaf prefers to communicate through sign language because it is perceived as their mother tongue and, in fact, it allows an immediacy of communication otherwise difficult to obtain. The current developments in information technology and the increase in the processing power of portable devices (in particular smartphones, handheld computers and other mobile devices) enabled us to think about the design of assistive technology that can make an automatic translation of text into sign language for the Deaf. As the processing power and energy consumption of portable devices are limited, appropriate solutions have to be explored to enable acceptable usability by the Deaf Community. This research achieved a working prototype that can translate natural language text (in this study, Italian) into Italian Sign Language (LIS). Moreover, a digital dictionary has been constructed and validated with the help of the Deaf. This dictionary extends the current state-of-the-art paper dictionary by more than 20% of terms [J15],[C27],[C26],[C25],[C23]. **Impact: some companies are now using our extended dictionary to provide LIS gesture rendering service for the deaf-community, thus increasing the availability of LIS.**

- **Innovative cache design techniques for designing embedded systems and for computer architecture education** The processing system internals contain many details which cannot be checked directly, such as the pipelines or the caches. Therefore, it is crucial to rely on experimental tools capable, on the one hand, understanding the inside of the microprocessor and the cache memory through simple (possibly web-based) visual tools and, on the other hand, enabling the teacher to monitor the student activities while he/she is exploring the complexity of the processor. This research has led to artefacts made publicly available to the international teaching community for Computer Architecture. Tools for simulating the MIPS and RISC-V pipelines through visualising the internal components and dynamic state while running actual programs have been provided. In this research, new tools were implemented. Interestingly, some of the features of those tools (such as the exploration of 3D locality curves) have been found useful also for the system designer and have been included in commercial tools such as the ChARM for the VLSI Technology Inc. "Jumpstart Kit" [J34],[J4],[C52],[C18],[C8],[C6][C5]. **Impact: visualization tools are key to system designers and for engineer education.**

6 Research Projects

R26. 2024-25 Role: **Coordinator(PI)** (ICSC - Italian Center for Super-Computing), "EDGE-ME - Data-Driven Methodologies for the Management of High-Performance Parallel Applications on Heterogeneous Architectures for Edge-Computing", (EUR 303'920 total funding, EUR **150'000** for UNISI).

R25. 2024-25 Role: **Partecipant** (ICSC - Italian Center for Super-Computing), "GEANT-HPC - Development and Optimization of GEANT4 for Space Experiments", (EUR 155'261 total funding, EUR **155'261** for UNISI).

R24. 2023-26 Role: **Local PI** (Horizon-Europe and Italian Ministry for Made in Italy), "BIREX plus plus - European Digital Innovation Hub", (EUR 5'995'583 total funding, EUR **114'383** for UNISI) - got Seal of Excellence.

R23. 2023-25 Role: **HPC Leader** (National Plan for Recovery and Resilience (PNRR)), "SAILS - Siena infrastructure for Artificial Intelligence and Life Science", (EUR 11'993'869 total funding, EUR **5'876'995** for UNISI) - ranked first among 25 projects, awarded but not executed.

R22. 2022-24 Role: **Coordinator(PI)** (Regione Toscana FSC), "High-Performance Artificial Intelligence Hardware Library" - DD21607/21 , (EUR 60'000 total funding, EUR **60'000** for UNISI).

R21. 2021-22 Role: **Coordinator(PI)** (Quest-IT), "Visualization of Signs for the Deaf by an Avatar", (EUR 30'000 total funding, EUR **30'000** for UNISI).

R20. 2015-2018 Role: **Coordinator(PI)** (European Commission - H2020), "AXIOM: Agile, eXtensible, fast I/O Module for the cyber-physical era" - project id. 645496, (EUR 3'945'937 total funding, EUR **985'000** for UNISI) - Selection Mark: 14.5/15.

R19. 2015-2018 Role: **Workpackage Leader WP7 "Evaluation and Design Space Exploration"** (European Commission - H2020), "AXIOM: Agile, eXtensible, fast I/O Module for the cyber-physical era" - project id. 645496.

R18. 2012-2014 Role: **Coordinator(PI)** (European Commission - Special FP7-FET objective for cooperating with non-EU partners), Future and Emerging Technologies - Large Project - TERAFLUX–INCO "Exploiting Dataflow Parallelism in Teradevice Computing in cooperation with University of Delaware, USA" - project id. 309229, (EUR 420'000 total funding, EUR **150'000** for UNISI) - Selection Mark: 15/15.

R17. 2010-2014 Role: **Workpackage Leader WP1 "Integration activities between TERAFLUX and UD"** (European Commission - FP7-FET), Future and Emerging Technologies - Large Project - "TERAFLUX – Exploiting Dataflow Parallelism in Teradevice Computing in cooperation with University of Delaware, USA" - project id. 309229.

R16. 2010-2014 Role: **Coordinator(PI)** (European Commission - FP7-FET), TERAFLUX: "Exploiting Dataflow Parallelism in Teradevice Computing" project id. 249013, (EUR 5'700'000 total funding, EUR **1'167'000** for UNISI) - Selection Mark: 15/15.

R15. 2010-2014 Role: **Workpackage Leader WP7 "Common Simulation and Compilation Platform"** (European Commission - FP7-FET), "TERAFLUX – Exploiting Dataflow Parallelism in Teradevice Computing" project id. 249013.

R14. 2010-2013 Role: **Workpackage Leader WP1 "Embedded Application Analysis"** (European Commission - FP7-ICT), ERA: "Embedded Reconfigurable Architecture" - project id. 249059, (EUR 2'800'000 total funding, EUR **417'000** for UNISI).

R13. 2010-2014 Role: **Participation** (HiPEAC networking funding), HIPEAC3: "High-Performance Embedded Architecture and Compilation", (EUR 4'000 total funding, EUR **4'000** for UNISI).

R12. 2008-2009 Role: **Coordinator(PI)** (Monte dei Paschi di Siena Foundation), "Integration of Sign Language for the Deaf in the digital television", (EUR 50'000 total funding, EUR **50'000** for UNISI).

R11. 2007-2008 Role: **Coordinator(PI)** (Regione Toscana - through National Association of the Deaf), "Extension of the digital vocabulary of an automated Sign Language System for the Deaf", (EUR 10'000 total funding, EUR **10'000** for UNISI).

R10. 2008-2012 Role: **Participation** (HiPEAC networking funding), HiPEAC Network of Excellence HIPEAC2: "High-Performance Embedded Architecture and Compilation", (EUR 5'000 total funding, EUR **5'000** for UNISI).

R9. 2008 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), HiPEAC Network of Excellence "Multithreaded Dataflow Architectures", (EUR 10'240 total funding, EUR **10'240** for UNISI).

R8. 2008 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), "Cache implications of non-blocking thread execution in a multithreaded architecture", (EUR 14'000 total funding, EUR **14'000** for UNISI).

R7. 2005-2009 Role: **Participation** (European Commission - FP6-FET), Future and Emerging Technologies - Integrated Project (IP) SCALA/SARC: "Scalable ARChitectures", (EUR 8'500'000 total funding, EUR **(through University of Pisa) 90'000** for UNISI).

R6. 2006 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), HiPEAC Network of Excellence "Scalable Multicore Architectures" in Cooperation with Universities of Goteborg-Chalmers (Sweden), Delft-TUD (Netherlands), Barcelona-UPC (Spain), (EUR 30'000 total funding, EUR **10'000** for UNISI).

R5. 2004-2008 Role: **Deputy Steering Committee** (European Commission - FP6-NoE), HiPEAC Network of Excellence "High-Performance Embedded Architecture and Compilation", coordination: Polytechnic University of Catalonia, Spain (UPC), (EUR 3'900'000 total funding, EUR **n/a** for UNISI).

R4. 2004-2005 Role: **Coordinator(PI)** (Italian Investment Fund for Basic Research (FIRB), Italian Ministry of Education, University and Research (MIUR)), "Innovative Architectures for High Performance Processors", (EUR 60'000 total funding, EUR **30'000** for UNISI).

R3. 2004 Role: **Coordinator(PI)** (Monte dei Paschi di Siena Foundation), "Study and Realization of a Multimedia System for Translating and Communicating with the Sign Language for the Deaf", (EUR 40'000 total funding, EUR **40'000** for UNISI).

R2. 2004-2005 Role: **Coordinator(PI)** (University Research Plan (PAR) of the University of Siena), "Innovative Architectures for Multimedia Applications in Embedded Systems", (EUR 15'000 total funding, EUR **15'000** for UNISI).

R1. 2003-2005 Role: **Participation** (Italian Investment Fund for Basic Research (FIRB), Italian Ministry of Education, University and Research (MIUR)), "Reconfigurable Platforms for Broadband Mobile Devices", activity of "Development of Innovative Cryptographic Techniques", coordinator prof. Enrico Martinelli, (EUR 320'000 total funding, EUR **80'000** for UNISI).

7 Journal Papers [statistics]

J39. R. Giorgi, M. Stojilovic, "Introduction to the ARC 2025 Journal Track", ***ACM Trans. Reconfigurable Technol. Syst.***, New York, NY, USA, vol. 19, no. 3, Sept. 2026, pp. 4, ISSN: 1936-7406, DOI: 10.1145/3839105.

J38. S. Hozhabr, R. Giorgi, "A Survey on Real-Time Object Detection on FPGAs", ***IEEE Access***, 2025, pp. 1-1, ISSN: 2169-3536, SCOPUS: 2-s2.0-85218803043, DOI: 10.1109/ACCESS.2025.3544515.

J37. Amin Sahebi and Marco Procaccini and Roberto Giorgi, "HashGrid: An optimized architecture for accelerating graph computing on FPGAs", ***Future Generation Computer Systems***, vol. 162, 2025, pp. 1-15, ISSN: 0167-739X, SCOPUS: 2-s2.0-85202938974, WOS:001306729600001, DOI: 10.1016/j.future.2024.107497.

J36. M. Procaccini, A. Sahebi, R. Giorgi, "A survey of graph convolutional networks (GCNs) in FPGA-based accelerators", ***Journal of Big Data***, vol. 163, no. 11, 11 Nov 2024, pp. 36, ISSN: 2196-1115, SCOPUS: 2-s2.0-85212210374, WOS:001352404900001, DOI: 10.1186/s40537-024-01022-4.

J35. A. Sahebi, M. Barbone, M. Procaccini, W. Luk, G. Gaydadjiev, R. Giorgi, "Distributed large-scale graph processing on FPGAs", ***Springer Journal of Big Data***, vol. 10, no. 1, Jun 2023, pp. 28, ISSN: 2196-1115, SCOPUS: 2-s2.0-85161084227, WOS:001000115000001, DOI: 10.1186/s40537-023-00756-x.

J34. G. Mariotti, R. Giorgi, "WebRISC-V: A 32/64-bit RISC-V pipeline simulation tool", ***ELSEVIER SoftwareX***, vol. 18, May 2022, pp. 1-7, ISSN: 2352-7110, SCOPUS: 2-s2.0-85130837344, WOS:000806618800002, DOI: 10.1016/j.softx.2022.1011

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P20. A. Sahebi, L. Verdoscia, R. Giorgi, "A Data-Flow Approach To Accelerate Real-Valued Fast Fourier Transform", *HiPEAC ACACES-2019*, Fiuggi, Italy, July 2019, pp. 155-158, (poster), ISBN: 978-88-905806-7-3.

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P14. M. Procaccini, R. Giorgi, "Simulation infrastructure for the next kilo x86-64 Chips", *HiPEAC ACACES-2017*, Fiuggi, Italy, Julyy 2017, pp. 91-94, (poster), ISBN: 978 88 905806 5 9.

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13 Technical Reports and Deliverables

D20. R. Giorgi, F. Khalili, F. Montefoschi, M. Procaccini, X. Martorell, D. Jiménez-González, A. C., P. Gai, S. Garzarella, V. Amourianos, D. Theodoropoulos, D. Pnevmatikatos, D. Oro, D. Catani, D. Cardillo, C. Magnani, S. Viola, N. Bettin, A. Pomella, "Performance and Energy Evaluation of AXIOM", *AXIOM D7.3*, Siena, Italy, Feb 2018, pp. 1-54, (deliverable).

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D1. R. Badia, Y. Etsion, J. Labarta, N. Navarro, M. Pavlovic, C. Servat. H. and Villavieja, S. Girbal, M. Ansari, M. Lujan, C. Kirkham, I. Watson, R. Giorgi, A. Portero, A. Cohen, "Rep. on the reference set of applications chosen, and initial characterization of the applications", *TERAFLUX D2.1*, Siena, Italy, Dec 2010, pp. 1-44, (deliverable).

14 Intellectual Property

IP2. S. Bartolini, P. Bennati, R. Giorgi, "BlueSign 2", *SIAE 24-02-2006/001*, Reg. 24 Feb. 2006.

IP1. P. Bennati, T. Capasso, V. Di Massa, F. Giallombardo, R. Giorgi, M. Guerrini, E. Maggio, N. Nannetti, "BlueSign Translator", *SIAE 002568, Ord. D003454*, Reg. 21 Mar. 2003.

15 Educational and Research Software

SW8. 2019(June)The WebRISC-V: Web-based RISC-V pipeline simulator http://www.dii.unisi.it/~giorgi/WebRISC-V

- Simulates a RISC-V pipeline inside a web browser. The architectural elements are visualized while instructions pass through the pipeline.
- This is a Bachelor Thesis that I supervised (Gianfranco Mariotti) for the realization of this tool, which led to a publication at the Workshop on Computer Architecture Education.

SW7. 2015(May) FREESS: The Free SuperScalar simulator http://www.dii.unisi.it/~giorgi/freess

- Simulates a simple Superscalar processor step-by-step, visualizing the activity of renaming, instruction window, reorder buffer, load/store queues.
- I am the author of this educational tool for students. The tool is written from scratch.

SW6. 2013(Sep) The Dataflow Run Time (DRT) http://sourceforge.net/projects/drt/

- A runtime library to code and debug programs that are based on a Thread-Level-Parallelism Instruction Set Extension (TLP ISE).
- I am the author of this tool which allows to execute programs in a dataflow style by simpling adding a header and using few library calls.

SW5. 2013(Jun) COTSon Thread Scheduler Unit (TSU) http://sourceforge.net/p/cotson/code/HEAD/tree/branches/timing-unisi/tsu4/

- A functional and timing model for an x86_64 based full-system. It uses a custom Instruction Set Extension (ISE) to support a dataflow based execution model. The model is a plugin of the HP-Labs COTSon full-system simulator.
- I coordinated a large group of more than ten researchers within the TERAFLUX project, by providing the core idea of a dataflow based scheduler, constant supervision and the leadership of the project.

SW4. 2010(Jun) The ERA BENCHMARK-SUITE http://www.dii.unisi.it/~giorgi/ebs

- A benchmark suite for research on embedded system for mobile.
- I coordinated a large group of more than ten researchers within the ERA project, by providing the core of a public set of benchmarks for embedded applications for mobile platforms, constant supervision and the leadership of the project.

SW3. 2004(May)The WEBMIPS: Web-based MIPS simulator http://www.dii.unisi.it/~giorgi/WEBMIPS and a revived version in PHP coming from the WebRISC-V project (see above) http://www.dii.unisi.it/~giorgi/WebMIPS

- Simulates a MIPS pipeline inside a web browser. The architectural elements are visualized while instructions pass through the pipeline.
- This started as a student project and I supervised the realization of this tool which led to a highly cited publication.
- The WebMIPS is a PHP edition of WEBMIPS (originally written in ASP), realized as part of a Bachelor thesis.

SW2. 2003(Sep) The BASICRYPT BENCHMARK-SUITE http://www.dii.unisi.it/~giorgi/basicrypt

- A benchmark suite for research on Elliptic Curve Cryptography.
- I coordinated a group of researchers within a FIRB project, by providing the core of a public set of benchmarks for cryptography based on Elliptic Curves.

SW1. 2003(June) JCACHESIM cache+CPU web-based simulator http://www.dii.unisi.it/~giorgi/jcachesim

- Simulates a cache memory and its internal operation, while executing simple MIPS programs. It runs in a java enabled web browser.
- This project originated from a Master thesis that I supervised and migrated from an old MS-DOS interface the full capabilities to a Java applet, while adding the cross-compilation of MIPS code.

16 Public Talks

T67. 2025(Jun), (FREESS: Free RISC-V inspired Superscalar Educational Simulator, WCAE/ISCA, Tokyo, Japan), "(presentation)"

T66. 2025(May), (Keynote Speech at 12th International BSC Severo Ochoa Doctoral Symposium 2025), "https://www.bsc.es/educati phd/doctoral-symposium/12th-international-bsc-severo-ochoa-doctoral-symposium-2025"

T65. 2025(Jan), (HashGrid: Optimized FPGA Architecture for Accelerating Graph Processing in Large-Scale Computing), "Workshop on Reconfigurable Computing" (Invited talk)

T64. 2025(Jan), (Reconfigurable Computing in the Age of RISC-V, OpenSource and Chiplets: Chances and Challenges), "Workshop on Reconfigurable Computing" (panelist)

T63. 2024(Jul), (Keynote Speech at International Symposium on High-Level Parallel Programming and Applications (HLPP-24), Pisa, Italy), " DataFlow-Threads (DF-Threads): An Execution Model for Scalable Systems " (presentation)

T62. 2024(Jan), (Invited Speech at Workshop on RISC-V for HPC, Munich, Germany), "WebRISC-V: A web-based educational simulator for visualising RISC-V pipeline content at runtime" (presentation)

T61. 2023(Sep), (Invited Speech at Workshop on Scalable Performance, Bertinoro, Italy), "A Proposal for Large-Scale Graph Processing on Multi-FPGAs" (presentation)

T60. 2023(Sep), (Italian Conference on Big Data and Data Science, Naples, Italy), "Accelerating Large-scale Graph Processing with FPGA-Based Distributed Computing" (presentation)

T59. 2023(Sep), (Bioinformatiha, Giornata Toscana di Bioinformatica e System Biology, Naples, Italy), "The SAILS projeject: an HPC system for Siena Artificial Intelligence and Life Science" (presentation)

T58. 2022(Sep), (Italian Workshop on High-Performance Computing, Turin, Italy), "SAILS: Siena infrastructure for Artificial Intelligence and Life Science" (presentation)

T57. 2022(Sep), (Italian Workshop on High-Performance Computing, Turin, Italy), "There's still plenty of room at the bottom for HPC" (presentation)

T56. 2022(Jun), (Workshop on Reconfigurable Computing, Budapest, Hungary), "Distributed Large-Scale Graph-Processing on FPGA" (Invited talk)

T55. 2022(Jun), (The future of FPGAs in AI: Is it Mission Impossible given the dedicated ASICs), "Workshop on Reconfigurable Computing" (panelist)

T54. 2022(Jun), (Workshop Nazionale per il trasferimento tecnologico e l'alta formazione, Verona, Italy), "Extending IoT across a cluster of FPGAs: the Gluon-board" (presentation)

T53. 2022(Jun), (Keynote Speech at IEEE MECO conference, Budva, Montenegro), "Extending Performance and Reliability via Modular FPGA Clusters" (Invited keynote talk)

T52. 2021(Sep), (Invited Speech at Workshop on Scalable Performance, Bertinoro, Italy), "Extending Performance and Reliability via Thread-Level Dataflow Management" (presentation)

T51. 2021(Feb), (Italian Workshop on Embedded Systems, Italy), "GLUON-B: A modular Board for FPGA clusters" (presentation)

T50. 2020(Jan), (Workshop on Reconfigurable Computing, Bologna, Italy), "Scalable Performance by Scaling Out FPGA Systems Via Inexpensive Interconnects and the Open-Source AXIOM Software Stack" (Invited talk)

T49. 2019(Sep), (Invited Speech at Workshop on Scalable Performance, Bertinoro, Italy), "A Lightweight Programming Model for a Data-Flow Execution Model" (presentation)

T48. 2019(Sep), (Italian Workshop on High Performance Computing, University of Bologna, Italy), "Data-Flow based HPC" (presentation)

T47. 2019(Jul), (High Performance Computing and Simulation Conference, Dublin, IE), "Bridging a Data-Flow Execution Model to a Simple Programming Model" (presentation)

T46. 2019(Jul), (Department of Computer Science, University of Pisa, Italy), "DataFlow-Threads (DF-Threads): An Execution Model for Scalable Systems " (presentation)

T45. 2019(Jun), (Workshop on Computer Architecture Education (WCAE-2019)), "WebRISC-V: a Web-Based Education-Oriented RISC-V Pipeline Simulation Environment" (presentation)

T44. 2019(Mar), (Conference on Design, Automation and Test in Europe (DATE-2019)), "AXIOM: A Scalable, Efficient and Reconfigurable Embedded Platform" (presentation)

T43. 2019(Feb), (IEEE Euromicro Int.l Conf. on Parallel, Distributed, and Network-Based Processing), "Analyzing the Impact of Operating System Activity of different Linux Distributions in a Distributed Environment" (presentation)

T42. 2019(Jan), (11th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools), "A Design Space Exploration Tool Set for Future 1K-core High-Performance Computers" (presentation)

T41. 2018(Sep), (Third Italian Workshop on Embedded Systems), "The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board" (presentation)

T40. 2018(Jan), (SHiP-CPS: Software-Hardware Platforms for Cyber-Physical Systems), "The AXIOM platform for Cyber-Physical Systems" (presentation)

T39. 2018(Sep), (Invited Speech at Workshop on Scalable Performance, Bertinoro, Italy), "Accelerating Dense Matrix Multiplication through DataFlow-Threads (DF-Threads)" (presentation)

T38. 2018(Jun), (Keynote Speech at IEEE MECO conference), "The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board" (Invited keynote talk)

T37. 2017(Sep), (Second Italian Workshop on Embedded Systems), "The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board" (presentation)

T36. 2016(Sep), (First Italian Workshop on Embedded Systems), "AXIOM: A 64-bit scalable embedded system including Arduino socket and on-chip FPGA" (presentation)

T35. 2016(Sep), (VIMAR, Marostica, Italy), "AXIOM Operating System analysis" (presentation)

T34. 2016(Jun), (Barcelona Supercomputing Center, Barcelona, Spain), "AXIOM Design Exploration Tools" (presentation)

T33. 2016(Apr), (ARTEMIS Spring Event, Vienna, Austria), "The AXIOM Cyber Physical System" (presentation)

T32. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), "The AXIOM project" (presentation)

T31. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), "The COTSon simulation environment" (tutorial)

T30. 2015(Feb), (CEA conference, Dubai, UAE), "Accelerating Haskell on a Dataflow Architecture: a case study including Transactional Memory"

T29. 2014(Oct), (MPP Workshop, Paris, France), "An Introduction to DF-Threads and their Execution Model"

T28. 2014(Sep), (Istituto di Calcolo ad Alte Prestazioni, Napoli, Italy), "TERAFLUX: Harnessing 1 TERA devices in a single package"

T27. 2013(Aug), (Georgia Tech, Atlanta, GA, USA), "TERAFLUX overview and the T* instruction extension"

T26. 2013(Aug), (University of Delaware, DE, USA), "TERAFLUX Research Overview"

T25. 2013(Oct), (SoC conference,Tampere,FI), "The TERAFLUX Project OVERVIEW" (presentation)

T24. 2013(Oct), (SoC conference,Tampere,FI), "MANY-CORE CHIPS and New High-Performance Computing Platforms: Hardware Thread-Level Parallelism Support in Many-Core Architectures" (tutorial)

T23. 2013(Jun), (CASTNESS workshop, Barcelona, Spain), "The T* Instruction Set Extension" (presentation)

T22. 2013(May), (University of Pisa, Italy), "DATAFLOW: different answer to achieve Scalabilty" (tutorial)

T21. 2013(Mar), (DATE Conference, Grenoble, France), "Lessons learned from European Projects" (Panel)

T20. 2013(Feb), (University of Siena, Italy), "Creation and Management a Large Scale search Project"

T19. 2012(Jun), (), "TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices"

T18. 2012(May), (Computing Frontiers conference, Cagliari, Italy), "TERAFLUX: Exploiting Dataflow Parallelism Teradevice Computing"

T17. 2012(Jun), (CASTNESS workshop, Paris, France), "TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices"

T16. 2011(Oct), (DFM Workshop, Galveston, TX, USA), "Data Flow Execution models" (panelist)

T15. 2011(Apr), (ODES workshop, CGO Conference, Chamonix, France), "TERAFLUX: exploiting DATAFLOW parallelism" (Keynote speech)

T14. 2011(Jan), (CASTNESS workshop, Rome, Italy), "Overview of a TERAFLUX-like Architecture"

T13. 2010(Jun), (International Forum on Multicores), "Integrating multicore research and the COTSon simulation platform"

T12. 2010(May), (HiPEAC Computing Week, Edinburgh UK), "TERAFLUX: exploiting DATAFLOW parallelism"

T11. 2005(May), (Dept. of Electronics and Information Systems, Ghent, Belgium), "Tiled Architectures for Embedded Systems"

T10. 2004(Oct), (Dept. of Computer Engineering, Delft, Olanda), "Non- Conventional Microprocessor Architectures"

T9. 2004(Sep), (HiPEAC Workshop, Juan les Pins, France), "Embedded-System Research Overview"

T8. 2003(Nov), (University of Pisa, Italy), "Non-Conventional Microprocessor Architectures"

T7. 2002(Jan), (SSGRRw-2002 Conference, L'Aquila, Italy), "Non-Conventional Microprocessor Architectures"

T6. 2001(Nov), (SGS-Thomson Advanced Research Laboratory, Milan, Italy), "Architetture Non-Convenzionali per Microprocessore"

T5. 2000(Apr), (University of Siena, Italy), "Introduzione alla Architettura Scheduled Data-Flow -SDF"

T4. 1999(May), (Dept. of Electrical and Computer Engineering, University of Alabama in Huntsville, AL, USA), "Scheduled Dataflow Architecture: problems and issues"

T3. 1998(May), (University of Belgrade, Serbia, Yugoslavia), "Simulating Composite Workloads on Shared-Bus Symmetric Multiprocessors"

T2. 1997(Sep), (Facoltà di Ingegneria, Università di Salerno, Benevento), "Trace Factory: a Hybrid Approach to Trace Generation for Performance Evaluation of Shared Bus Multiprocessors"

T1. 1997(Aug), (Computer Science and Engineering Dept., University of Texas at Arlington, TX, USA), "Trace Driven Simulation of Shared-Bus Multiprocessors"

17 Supervised Collaborators/Students

1. Visiting Professor
   - 2012(Sep)-2014(May) Bruce Jacob (University of Maryland) - under coordination contract directed by Prof. Giorgi, on the TERAFLUX project.
2. Researchers
   - 2021(Nov)-2024(Jan) Marco Procaccini
   - 2012(Apr)-2014(Jan) Alberto Scionti
   - 2012(Apr)-2013(Apr) Marco Solinas
3. Postdocs
   - 2022(Jul)-current Hani Seyed Hozhabr
   - 2020(Nov)-2021(Oct) Farnam Khalili Maybodi
   - 2019(Apr)-2021(Jun) Marco Procaccini
   - 2010(Jun)-2013(Jul) Antonio Portero
   - 2012(Mar)-2013(Oct) Stamatis Kavvadias
   - 2010(Jun)-2012(Jan) Yu Zhibin
   - 2011(Sep)-2011(Dec) Sylvain Collange
   - 2010(Jun)-2011(May) Rania Mameesh
   - 2010(Jan)-2011(Jan) Vincenzo Di Massa
   - 2010(Jan)-2011(Jan) Nikola Puzovic
   - 2010(Apr)-2010(Jun) Andrea Casaccino
   - 2007(Oct)-2008(Nov) Paolo Bennati
4. Ph.D. Students
   - 2022(Nov)-current Tutoring of Ph.D. student Hani Seyed Hozhabr, ciclo XXXVII - Thesis title: "High-Performance and Efficient Artificial Intelligence Hardware Libraries"
   - 2018(Nov)-2022(Jun) Tutoring of Ph.D. student Amin Sahebi, ciclo XXXIV - Thesis title: "Reconfigurable Architectures for Accelerating Distributed Applications"
   - 2017(Oct)-2020(Sep) Tutoring of Ph.D. student Farnam Khalili Maybodi, ciclo XXXIII - Thesis title: "A Data-Flow Threads Co-processor for MPSoC FPGA Clusters"
   - 2016(Oct)-2019(Sep) Tutoring of Ph.D. student Marco Procaccini, ciclo XXXII - Thesis title: "A Data-Flow Execution Engine for Scalable Embedded Computing"

- 2013(Nov)-2017(Jul) Tutoring of Ph.D. student Somnath Mazumdar, ciclo XXIX - Thesis title: "An Efficient NoC-based Framework to Improve Dataflow Thread Management at Runtime"
- 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Nikola Puzovic, ciclo XXI - Thesis title: "Implementing fine/medium grained TLP support in multi-core architectures"
- 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Zdravko Popovic, ciclo XXI - Thesis title: "Multithreaded Dataflow in Tiled Architectures"
- 2004(Nov)-2007(Sep) Tutoring of Ph.D. student Paolo Bennati, ciclo XX - Thesis title: "Embedded Systems: Low-Power techniques and applications"
- 2001(Nov)-2005(Apr) Co-Tutoring of Ph.D. Student Irina Branovic - Thesis title: "Architectural Support for Elliptic Curve Cryptography (ECC) "

5. Graduate Students
   - 2021(Sep)-2022(Jun) Tutoring of student Gianfranco Mariotti (Bluesign)
   - 2020(Oct)-2021(Jul) Tutoring of student Gianfranco Mariotti (RISC-V)
   - 2017(Sep)-2017(Oct) Tutoring of student Farnam Khalili Maybodi
   - 2016(Dec)-2017(Feb) Hosting of Ph.D. student Arthur Lorenzon, from UFRGS, Brazil - sponsored by a 3-month HiPEAC (H2020) mobility grant.
   - 2014(Nov)-2015(Oct) Tutoring of Ph.D. student Nitin Satpute, ciclo XXX.
   - 2012(Jan)-2014(Nov) Tutoring of Ph.D. student Cai Kang, ciclo XXVII.
   - 2014(Aug)-2014(Nov) Tutoring of student Amit Fuchs
   - 2013(Jul)-2014(Mar) Tutoring of student Haileyesus Kifle
   - 2013(Nov)-2014(Mar) Tutoring of student Daniele Colobraro
   - 2013(Apr)-2014(Jan) Tutoring of student Bogdan Azaric
   - 2012(Jun)-2012(Nov) Tutoring of student Eliana Sala Mariet
   - 2012(Jun)-2013(Aug) Tutoring of student Andrea Mondelli
   - 2012(Jan)-2013(Apr) Tutoring of student Ho Nam
   - 2010(Jul)-2011(Jan) Tutoring of student Caroline Concatto
   - 2008(Sep)-2009(Jun) Tutoring of student Andrea Righi
   - 2008(Feb)-2008(Sep) Tutoring of student Nenad Korolija
   - 2008(Feb)-2008(Sep) Tutoring of student Roberto D'Aprile
   - 2004(Sep)-2005(Oct) Tutoring of student Zdravko Popovic
   - Orientation Activity for potential students coming from High School.
   - Tutor for several Master Thesis, Faculty of Engineering, University of Siena.

6. Master and Bachelor Students
   - 2024 Joel Alex Chuani Temawe (Bachelor), "Accelerazione delle prestazioni di Applicationi di Intelligenza Artificiale su Processore RISC-V".
   - 2022 Lorenzo Sacchi (Bachelor), "Implementazione di un Avatar per la Visualizzazione e Animazione di Gesti come Applicazione Lato Browser".
   - 2019 Gianfranco Mariotti (Bachelor), "Un Ambiente di Simulazione Accessibile via Web per lo Studio della Pipeline del Processore RISC-V".
   - 2015 Ettore Chimenti (Bachelor), "Porting di un sistema operativo GNU/Linux su Single-board computer ARM".
   - 2007 Giovanni Burresi (Bachelor), "Valutazione delle prestazioni di IBM Cell Processor nelle simulazioni finanziarie".
   - 2005 Fabio Antonio Cassini (Master), "Realizzazione del modulo aggiuntivo per un concentratore seriale su interfacce I^2C BUS e 1-wire bus".
   - 2005 Gian Lorenzo Meocci (Bachelor), "Studio e implementazione di un sistema embedded adibito al controllo del traffico".
   - 2004 Mauro Marchetti (Master), "Realizzazione di un sistema di supporto alle decisioni per investimenti in borsa basato su analisi tecnica e analisi delle notizie".
   - 2004 Christos Ververidis (Master), "Analisi delle prestazioni di sistemi di elaborazione con cache: uno strumento visuale".
   - 2001 Lorenzo Menconi (Master), "Progettazione di un sistema di supporto alle decisioni per l'investimento finanziario" (co-advisor).

18 Professional Activities

1. Founded initiatives
   - 2024 Promoter and Representative for the membership of the University of Siena in the RISC-V Foundation.
   - 2017 Founding member of the IEEE Special Technical Community "Parallel Model & System: Dataflow and beyond"
2. Project Evaluator
   - Rapporteur and Independent Expert of the European Commission for the evaluation of EuroHPC Project NET4EXA, May 2025.
   - Monitoring Committee Member for the CINI Laboratory on Big Data, June 2024.
   - Independent Expert of the European Commission for the evaluation of EuroHPC Project OPTIMA, January 2024.
   - Independent Expert of the European Commission for the evaluation of H2020 HPC Projects ENERXICO and ESCAPE2, October 2021.
   - Independent Expert of the MIUR under the REPRISE database for evaluation of Fundamental Research and Industrial Research, June 2018.
   - Independent Expert for the evaluation of PRIN projects (Italian Projects of National Relevance) since 2018.
   - Independent Expert of the European Commission for the evaluation of CHIST-ERA (Future and Emerging Technology) 2012 - FP7 (7th Framework Programme) March 2012.
   - Independent Expert of the European Commission for the evaluation of Call FET (Future and Emerging Technology) 2008 - FP7 (7th Framework Programme) Massive ICT. FP6 IST-FET-26825 SHAPES (Scalable Software Hardware Architecture Platform for Embedded Systems), November 2006 through January 2010.
   - Reviewer of NWO Projects (Netherlands Research Organization) and EU projects.
   - Consultant for the EU Call Objective ICT-2009.8.1: FET proactive 1: Concurrent Tera-device Computing, Brussels, Nov. 2008.
   - IEEE Judge (among the 8 coming from the Industry and the Academy) for IEEE Computer Science International Design Competition (CSIDC) 2001 (http://computer.org/csidc) sponsored by Intel, Toshiba, Ericsson, AMD, Microsoft, Lucent, EMC, Hewlett-Packard, Sun, Motorola, to assign prizes for 70'000 USD. June-July 2001.
3. Member of Ph.D. Graduation Committees
   - PhD External Evaluator:Universitat Politecnica de Catalunya, Barcelona, Spain, September 2026.
   - PhD Committee:Universitat Politecnica de Catalunya, Barcelona, Spain, July 2026.
   - PhD External Evaluator:Universitat Politecnica de Catalunya, Barcelona, Spain, March 2026.
   - PhD Committee:Scuola Superiore S. Anna, Pisa, Pisa, Italy, April 2025.
   - PhD External Evaluator:Scuola Superiore S. Anna, Pisa, Pisa, Italy, January 2025.
   - PhD External Evaluator:University of Naples, Federico II, Napoli, Italy, January 2025.
   - PhD Jury President:University of Florence, Florence, Italy, April 2023.
   - PhD External Evaluator:Istituto Nazionale di Fisica Nucleare, Rome, Italy, November 2020.
   - PhD Committee:Università di Pisa, Italy, Pisa, Italy, May 2020.
   - PhD Committee (2 candidates):Università degli Studi di Padova, Italy, Milan, Italy, October 2019.
   - PhD Committee (4 candidates):Politecnico di Milano, Milan, Italy, February 2019.
   - PhD External Evaluator:Istituto Nazionale di Fisica Nucleare, Rome, Italy, December 2017.
   - PhD External Evaluator:Universitat Politecnica de Valencia, Valencia, Spain, December 2016.
   - PhD Committee:Universitat Politecnica de Valencia, Valencia, Spain, December 2014.
   - PhD Committee:Universitat Politecnica de Catalunya, Barcelona, Spain, May 2014.
   - PhD Committee:Universitat Politecnica de Catalunya, Barcelona, Spain, September 2011.
   - PhD Committee:Chalmers University, Goteborg, Sweeden, June 2011.
   - PhD Committee:Universitat Politecnica de Catalunya, Barcelona, Spain, December 2009.
   - PhD Committee:IMT - Institute for Advanced Studies, Lucca, Italy, July 2009.
4. Member of Ph.D. Selection Committees
   - University of Florence, University of Pisa, University of Siena, "Smart Computing", Aug. 2022.
   - University of Florence, University of Pisa, University of Siena, "Smart Computing", Sept. 2015.

- University of Siena, Dept. of Information Engineering, Sept. 2010.
- University of Siena, Dept. of Information Engineering, Sept. 2008.

5. Journal Editorial Boards
   - 2026(Sep)-present Associate Editor of ACM Transactions on Architecture and Code Optimization (ACM-TACO).
   - 2025(Mar)-present Associate Editor of ELSEVIER Sustainable Computing (SUSCOM).
   - 2024(Aug)-present Member of the Editorial Board of SpringerNature International Journal of Networked and Distributed Computing (IJNDC).
   - 2019(Mar)-present Executive Editor of the International Journal of Embedded Systems (IJES).
   - 2017(Mar)-present Associate Editor of the International Journal of Embedded Systems (IJES).
   - 2014(Jan)-present Member of the editorial board of the International Journal of Embedded Systems (IJES).
   - Co-Guest Editor of ACM Computer Architecture News (official Newsletter of ACM Special Interest Group on Computer Architecture), number of December 2001, with emphasis on Compilation Techniques, Parallel Architectures and Frontiers Topics.
   - Guest Editor of IEEE-TCCA NEWSLETTER (official Newsletter of IEEE Special Interest Group in Computer Architecture), number of January 2001, with emphasis on MEmory DEcopupled Architectures in modern microprocessors.
   - Co-Guest Editor of Journal of Embedded Computing, 2006 special issue on Embedded Single-Chip Multicore Architectures and related research - from System Design to Application Support.
   - Journal Reviewer: IEEE Transaction on Computers, IEEE Transaction on Parallel and Distributed Systems, IEEE Micro, IEEE Concurrency, Computer Journal, Journal of System Architecture, IEEE Transaction on Circuits and Systems, Elsevier Microprocessor and Microsystems, ACM Transactions on Architecture and Code Optimization (TACO), Concurrency and Computation: Practice and Experience, Elsevier Parallel Computing, Journal of Parallel and Distributed Computing (JPDC).

6. Keynote Speaker
   - **Keynote Speaker**: 12th International BSC Severo Ochoa Doctoral Symposium 2025, Barcelona, Spain, May 2025.
   - **Keynote Speaker**: International Symposium on High-Level Parallel Programming and Applications, Pisa, Italy, July 2024.
   - **Keynote Speaker**: IEEE MECO Conference 2022, Budva, Montenegro, June 2022.
   - **Keynote Speaker**: IEEE MECO Conference 2017, Bar, Montenegro, June 2017.
   - **Keynote Speaker**: (ODES workshop, CGO Conference), "TERAFLUX: exploiting DATAFLOW parallelism", Chamonix, France, April 2011.
   - **Keynote Speaker**: SSGRR 2002w International Conference, L'Aquila, Italy, January 2002.

7. Chairing
   - **Program Co-Chair**: Applied Reconfigurable Computing Symposium, Seville, Spain, April 2025.
   - **Program Co-Chair**: 3rd Italian Workshop on HPC, Turin, Italy, September 2022.
   - **Program Chair**: 3rd Italian Workshop on Embedded Systems, IWES-2018, Siena, Italy, September 2018.
   - **Program Chair**: Software/Hardware platforms for Cyber-Physical Systems Workshop, Manchester, UK, January 2018.
   - **General Chair**: ACM Computing Frontiers 2017, Siena, Italy, May 2017.
   - **Program Chair** of the European-Project track: DATE 2016, Dresden, Germany, March 2016.
   - **General Chair**: CASTNESS 2012, Paris, France, January 2012.
   - **General Co-Chair**: HiPEAC WRC 2011, Heraklion, Greece, January 2011.
   - **Program Co-Chair**: HiPEAC WRC 2010, Pisa, Italy, January 2010.
   - Publicity Chair: HiPEAC 2010, Pisa, Italy, January 2010.
   - Financial/Local Co-Chair: WAIFI-2008 Workshop, Siena, Italy, July 2008.
   - **Program Co-Chair**: ESA-05 Conference, Las Vegas, Nevada, USA, June 2005.
   - **General Chair**: MEDEA-2001 Workshop, Barcelona, Spain (EU), September 2001.
   - **Program Chair**: MEDEA-2000 Workshop, Philadelphia, Pennsylvania (USA), October 2000.
   - **General Chair and Founder**: MEDEA-2000 Workshop, Philadelphia, Pennsylvania (USA), October 2000.

8. Program Committee Membership

PC177. DATE 2026, Verona, Italy, March 2026.
PC176. SBACPAD-2025, Bonito, MS, Brazil, October 2025.
PC175. Field Programmable Logic Conference, FPL-2025, Leiden, Netherlands, September 2025.
PC174. The 4th Italian Conference on Big Data and Data Science, ITADATA-2025, Turin, Italy, September 2025.
PC173. ICPP Embedded Multicore Systems, EMS 2025, Sand Diego, CA, USA, September 2025.
PC172. IEEE MECO CPS & IoT, Budva, Montenegro, June 2025.
PC171. EUROMICRO European Projects in Digital System Design, Salerno, Italy, May 2025.
PC170. EUROMICRO DSD-2025, Salerno, Italy, May 2025.
PC169. Architecture of Computing Systems, ARCS 2025, Kiel, Germany, April 2025.
PC168. International Symposium Applied Reconfigurable Computing, ARC 2025, Seville, Spain, April 2025.
PC167. HiPEAC RAPIDO 2025, Barcelona, Spain, January 2025.
PC166. The 3rd Italian Conference on Big Data and Data Science, ITADATA-2024, Pisa, Italy, September 2024.
PC165. Workshop on Virtualization in High-Performance Cloud Computing, VHPC-2024, Madrid, Spain, August 2024.
PC164. EUROMICRO European Projects in Digital System Design, Paris, France, August 2024.
PC163. EUROMICRO DSD-2024, Paris, France, August 2024.
PC162. ICPP Embedded Multicore Systems, EMS 2024, Gotland, Sweden, August 2024.
PC161. IEEE MECO CPS & IoT, Budva, Montenegro, June 2024.
PC160. Architecture of Computing Systems, ARCS 2024, Potsdam, Germany, May 2024.
PC159. International Symposium Applied Reconfigurable Computing, ARC 2024, Aveiro, Portugal, March 2024.
PC158. HiPEAC RAPIDO 2024, Munich, Germany, January 2024.
PC157. SBACPAD-2023, Porto Alegre, Brazil, October 2023.
PC156. Applied Reconfigurable Computing, ARC 2023, Cottbus, Germany, September 2023.
PC155. ICPP Embedded Multicore Systems, EMS 2023, Salt Lake City, Utah, USA, August 2023.
PC154. Architecture of Computing Systems, ARCS 2023, Athens, Greece, June 2023.
PC153. IEEE MECO CPS & IoT, Budva, Montenegro, June 2023.
PC152. 18th Workshop on Virtualization in High-Performance Cloud Computing, Hamburg, Germany, May 2023.
PC151. EUROMICRO European Projects in Digital System Design, Durres, Albania, September 2023.
PC150. EUROMICRO DSD-2023, Durres, Albania, September 2023.
PC149. HiPEAC RAPIDO 2023, Toulouse, France, January 2023.
PC148. Architecture of Computing Systems, ARCS 2022, Heilbronn, Germany, September 2022.
PC147. EUROMICRO European Projects in Digital System Design, Maspalomas, Gran Canaria, Spain, September 2022.
PC146. EUROMICRO DSD-2022, Maspalomas, Gran Canaria, Spain, September 2022.
PC145. ICPP Embedded Multicore Systems, EMS 2022, Bordeaux, France, August 2022.
PC144. International Symposium Applied Reconfigurable Computing, ARC 2022, Beijing, China, September 2022.
PC143. IEEE MECO CPS & IoT, Budva, Montenegro, June 2022.
PC142. IEEE COMPSAC 2022- Conference on Computers, Software, and Applications, Virtual Event, June 2022.
PC141. Field Programmable Logic Conference, FPL-2022, Belfast, UK, August 2022.
PC140. HiPEAC RAPIDO 2022, Budapest, Hungary, January 2022.
PC139. ICPP Embedded Multicore Systems, EMS 2021, Chicago, Illinois, USA, August 2021.
PC138. EUROMICRO DSD-2021, Palermo, Italy, September 2021.
PC137. IFIP Network and Parallel Computing, NPC-2021, Paris, France, July 2021.
PC136. IEEE DFM-2021, Virtual, July 2021.
PC135. Field Programmable Logic Conference, FPL-2021, Dresden, DE, September 2021.
PC134. Architecture of Computing Systems, ARCS 2021, Virtual, June 2021.
PC133. Applied Reconfigurable Computing, ARC 2020, Rennes, France, June 2021.
PC132. IEEE MECO CPS & IoT, Budva, Montenegro, June 2021.
PC131. HiPEAC RAPIDO 2021, Budapest, HU, January 2021.
PC130. HiPEAC WRC 2021, Budapest, HU, January 2021.
PC129. IEEE BIGDATASE-2020, Guangzhou, China, November 2020.
PC128. Field Programmable Logic Conference, FPL-2020, Goteborg, SW, September 2020.
PC127. ICPP Embedded Multicore Systems, EMS 2020, Edmonton, Canada, August 2020.
PC126. EUROMICRO DSD-2020, Portoroz, Slovenia, August 2020.
PC125. IEEE DFM-2020, Madrid, Spain, July 2020.
PC124. Workshop on Parallel Programming Models,, MPP 2020, New Orleans, Loiusiana, USA, May 2020.
PC123. Architecture of Computing Systems, ARCS 2020, Aachen, Germany, May 2020.
PC122. Applied Reconfigurable Computing, ARC 2020, Toledo, Spain, April 2020.
PC121. ACM SAC-2020 Special Track, Brno, Czech Republic, April 2020.
PC120. HiPEAC RAPIDO 2020, Bologna, IT, January 2020.
PC119. HiPEAC WRC 2020, Bologna, IT, January 2020.
PC118. IEEE DFM-2019, Milwaukee, Wisconsin, USA, July 2019.
PC117. Field Programmable Logic Conference, FPL-2019, Barcelona, Spain, September 2019.
PC116. EUROMICRO DSD-2019, Kallithea, Chalkidiki, Greece, August 2019.
PC115. ICPP Embedded Multicore Systems, EMS 2019, Kioto, Japan, August 2019.
PC114. The 8th International Workshop on Advances in Parallel Programming Models and Frameworks for the Multi-/Many-core Era, Dublin, Ireland, July, 2019.
PC113. IEEE MECO-2019, Budva, Montenegro, June 2019.
PC112. Architecture of Computing Systems, ARCS 2019, Copenhagen, Denmark, May 2019.
PC111. Applied Reconfigurable Computing, ARC 2019, Darmstadt, Germany, April 2019.

PC110. HiPEAC RAPIDO 2019, Valencia, ES, January 2019.
PC109. ACM SAC-2019 Special Track, Limassol, Cyprus, April 2019.
PC108. The 18th IEEE International Conference on Scalable Computing and Communications, ScalCom-2018, Guangzhou, China, October 2018.
PC107. IEEE ReConFig 2018, Cancun, Maxico, December 2018.
PC106. Field Programmable Logic Conference, FPL-2018, Dublin, Ireland, August 2018.
PC105. ICPP Embedded Multicore Systems, EMS 2018, Eugene, Oregon, USA, August 2018.
PC104. EUROMICRO DSD-2018, Prague, Czech Republic, August 2018.
PC103. IEEE MECO-2018, Budva, Montenegro, June 2018.
PC102. Applied Reconfigurable Computing, ARC 2018, Santorini, May 2018.
PC101. ACM SAC-2018 Special Track, Pau, France, April 2018.
PC100. Architecture of Computing Systems, ARCS 2018, Braunschweig, Germany, April 2018.
PC99. HiPEAC RAPIDO 2018, Manchester, UK, January 2018.
PC98. HiPEAC WRC 2018, Manchester, UK, January 2018.
PC97. IEEE ReConFig 2017, Cancun, Mexico, December 2017.
PC96. SBACPAD-2017, Campinas, Brazil, October 2017.
PC95. IEEE FPL-2017, Ghent, Belgium, September 2017.
PC94. ICPP Embedded Multicore Systems, EMS 2017, Bristol, UK, August 2017.
PC93. IEEE MSPDS 2017, Genova, Italy, July 2017.
PC92. IEEE MECO-2017, Bar, Montenegro, June 2017.
PC91. ACM SAC-2017 Special Track, Marrakesh, Morocco, April 2017.
PC90. Applied Reconfigurable Computing, ARC 2017, Delft, Netherlands, April 2017.
PC89. Architecture of Computing Systems, ARCS 2017, Vienna, Austria, April 2017.
PC88. HiPEAC Embedded 2017, Nurnberg, February 2017.
PC87. HiPEAC RAPIDO 2017, Stockholm, Sweden, January 2017.
PC86. HiPEAC WRC WRC 2017, Stockholm, Sweden, January 2017.
PC85. ICPP Embedded Multicore Systems, EMS 2016, Philadelphia, PA, USA, August 2016.
PC84. IEEE ReConFig 2016, Cancun, Mexico, November 2016.
PC83. IEEE DFM-2016, Haifa, Israel, September 2016.
PC82. IEEE FPL-2016, Lausanne, Switzerland, August 2016.
PC81. IEEE MECO-2016, Bar, Montenegro, June 2017.
PC80. ACM SAC-2016 Special Track, Pisa, Italy, April 2016
PC79. IEEE MSPDS 2016, Innsbruck, Austria, July 2016.
PC78. Architecture of Computing Systems, ARCS 2016, Nurnberg, April, 2016.
PC77. HiPEAC WRC 2016, Prague, Czech Republic, January 2016.
PC76. HiPEAC RAPIDO 2016, Prague, Czech Republic, January 2016.
PC75. IEEE DFM-2015, San Francisco, CA, USA, October 2015.
PC74. IEEE ICCD-2015, New York, USA, October 2015.
PC73. IEEE FPL-2015, London, UK, September 2015.
PC72. IEEE WCS-IOT 2015, London, UK, September 2015.
PC71. EUROMICRO DSD-2015, Funchal, Madeira, Portugal, August 2015.
PC70. IEEE M2A2-2015, New York, USA, August 2015.
PC69. WRC-2015 Workshop, Amsterdam, Netherlands, January 2015.
PC68. MULTIPROG-2015 Workshop, Amsterdam, Netherlands, January 2015.
PC67. ARCS-2015, Porto, Portugal, March 2015.
PC66. ACM SAC-2015 Special Track, Salamanca, Spain, April 2015.
PC65. IEEE ICPADS-2014, Hsinchu, Taiwan, December 2014.
PC64. IEEE ICCD-2014, Seoul, Korea, October 2014.
PC63. IEEE FPL-2014, Munich, Germany, September 2014.
PC62. IEEE DFM-2014, Edmonton (Alberta), Canada, August 2014.
PC61. IEEE M2A2-2014, Paris, France, August 2014.
PC60. 2014 ACM International Conference on Supercomputing (ICS), (External Review Committee), Munich, Germany, June 2014.
PC59. ACM SAC-2014 Special Track, Gyeongiu, South Korea, March 2014.
PC58. ARCS-2014, Lubeck, Germany, February 2014.
PC57. MULTIPROG-2014 Workshop, Vienna, Austria, January 2014.
PC56. IEEE ICPADS-2013, Seoul, Korea, December 2013.
PC55. IEEE ICCD-2013, Asheville, NC, USA, October 2013.
PC54. IEEE DFM-2013, Edinburgh, UK, September 2013.
PC53. IEEE FPL-2013, Porto, Portugal, August 2013.
PC52. IEEE M2A2-2013, Melbourne, Australia, July 2013.
PC51. HiPEAC WRC 2013, Berlin, Germany, January 2013.
PC50. ACM SAC-2013 Special Track, Trento, Italy, March 2013.
PC49. ARCS-2013, Prague, Czech Republic, February 2013.
PC48. MULTIPROG-2013 Workshop, Berlin, Germany, January 2013.
PC47. IEEE FPL-2012, Oslo, Norway, August 2012.
PC46. IEEE M2A2-2012 Workshop IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms, Madrid, Spain, July 2012.

PC45. IEEE ICCD-2012, Montreal, Quebec, Canada, September 2012.
PC44. Workshop on the Growing Problems with Scalable Heterogeneous Infrastructures (GSHI'12), Madrid, Spain, July 2012.
PC43. HiPEAC WRC 2012, Paris, France, January 2012.
PC42. ACM SAC-2012 Special Track, Trento, Italy, March 2012.
PC41. ARCS-2012, Munich, Germany, February 2012.
PC40. MULTIPROG-2012 Workshop, Paris, France, January 2012.
PC39. IEEE SEC-2011, Sydney, Australia, December 2011.
PC38. IEEE ICCD-2011, Amherst, MA, USA, October 2011.
PC37. IEEE FPL-2011, Chania, Greece, September 2011.
PC36. ACM SAC-2011 Special Track, TaiChung, Taiwan, March 2011.
PC35. ARCS-2011, Lake Como, Italy, February 2011.
PC34. MULTIPROG-2011 Workshop, Heraklion, Greece, January 2011.
PC33. IEEE ICCD-2010, Amsterdam, Netherlands, October 2010.
PC32. IEEE FPL-2010, Milano, Italy, August 2010.
PC31. MULTIPROG-2010 Workshop, Pisa, Italy, January 2010.
PC30. ACM SAC-2010 Special Track, Sierre, Switzerland, March 2010.
PC29. IEEE ICCD-2009, Lake Tahoe, California (USA), October 2009.
PC28. WoRMES 2009, Vancouver, Canada, August 2009.
PC27. ICPP 2009, Vienna, Austria, September 2009.
PC26. Computing Frontiers 2009, Ischia, Italy, May 2009.
PC25. ACM SAC-2009 Special Track, Honolulu, Hawaii (USA), March 2009.
PC24. MULTIPROG-2009 Workshop, Paphos, Cyprus, January 2009.
PC23. IEEE ICCD-2008, Lake Tahoe, California (USA), October 2008.
PC22. MEDEA-2008 Workshop, Toronto, Canada, October 2008.
PC21. IEEE SEC-2008, Beijing, China, October 2008.
PC20. MEDEA-2008 Workshop, Toronto, Canada, October 2008.
PC19. IEEE SEC-2008, Beijing, China, October 2008.
PC18. ACM SAC-2008 Special Track, Fortaleza, Brazil, March 2008.
PC17. MULTIPROG-2008 Workshop, Goteborg, Sweden, January 2008.
PC16. MEDEA-2007 Workshop, Brasov, Romania, September 2007.
PC15. HiPEAC 2007 Conference , Ghent, Belgium, January 2007.
PC14. ACM SAC-2007 Special Track, Seoul, Korea, March 2007.
PC13. MEDEA-2006 Workshop, Seattle, Washington, USA, September 2006.
PC12. ACM SAC-2006 Special Track, Dijon, France, April 2006.
PC11. HiPEAC 2005 Conference , Barcelona, Spain, November 2005.
PC10. MEDEA-2005 Workshop, Saint Loius, Missouri, USA, September 2005.
PC9. SCOPES-2005 Workshop, Dallas, Texas, USA, September 2005.
PC8. PDES-05 IEEE/IFIP Workshop, Fukuoka, Japan, July 2005.
PC7. ACM SAC-2005 Special Track, Santa Fe, New Mexico, USA, March 2005.
PC6. MEDEA-2004 Workshop, Antibes Juan-les-Pins, France, September 2004.
PC5. ACM SAC-2004 Special Track, Nycosia, CIPRO, March 2004.
PC4. MEDEA-2003 Workshop, New Orleans, Louisiana (USA), September 2003.
PC3. ACM SAC-2003 Special Track, Melbourne, Florida (USA), March 2003.
PC2. PACT-2002 Conference, Charlottesville, Virginia (USA), September 2002.
PC1. MEDEA-2002 Workshop, Charlottesville, Virginia (USA), September 2002.

19 Major Departmental Committees

- 2024(Mar)-present **University of Siena representative in the RISC-V foundation**.
- 2020(Apr)-present **National Deputy of the University of Siena** in the Italian Group of Informatics Engineering (GII).
- 2018(Oct)-present **Scientific Director of the University of Siena** in the Italian Academic Consortium for Informatics (CINI).
- 2018(Oct)-present **Delegate of the University of Siena (appointed by the Ministry)** in the Italian Academic Consortium for Informatics (CINI).
- 2015(Jun)-present **Member of Ph.D. Committee "Smart Computing"** (Uni. of Florence, Pisa, Siena).
- 2022(Feb)-present Department delegate for the Technological/Scientific Library Committee of the University of Siena.
- 2000-present President and member of several selection procedure for Researchers (5 times), Ph.D. grants (4 times), Postdoc grants (10+ times), Post-laurea grants (11+ times).

- 2014-2018 Member of the Student Tutoring Committee for the University of Siena.
- 2010-2018 Member of Admission Committee to the Master Degrees.
- 2018(Mar)-2021(Oct) Department Deputy for the University of Siena Alumni Association.
- 2019(Jan)-2021(Oct) Member of the Orientation commission.
- 2012(Nov) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2012-2015 Member of Department Committee for the Management of Scientific spaces.
- 2006 **President** of the Self-Evaluation Committee (RAV) for the Information Engineering Laurea.
- 2002-2010 Member of Ph.D. Committee (Department of Information Engineering, Siena).
- 2001-2010 Member of Local Area Network Management (Department Information Engineering, Siena).
- 2006-2009 Member of the Evaluation Board (**Comitato Didattica**) for **Master Degree (Laurea Specialistica)** in Computer Engineering (Faculty of Engineering, Siena).
- 2006-2009 Member of the Evaluation Board (**Comitato Didattica**) for **Bachelor Degree (Laurea Triennale)** in Computer Engineering (Faculty of Engineering, Siena).
- 2001-2009 Member of the Evaluation Board (**Comitato Didattica**) for Master in New Technologies and Company Management (University of Siena).
- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2005(Oct) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2000-2005 Member of the Orientation and Tutoring commission.
- 2000-2005 Design and Maintenance of Orientation WEB Site, Faculty Engineering, Siena (www.ing.unisi.it/orientamento - www.ing.unisi.it/orientamento/initinere - www.ing.unisi.it/orientaing).

20 Teaching

The following courses have been taught at the University of Siena at the School of Engineering, at the School of Economics and at the S.Chiara College. From year 2000 until now, more than 425 ECTS credits[1] have been taught (corresponding to an average of about 17 credits per year).

As Associate Professor:

Year	Course	ECTS credits	Level	School	Lang.
2025-2026	Advanced Computer Architecture	9	Master	Information Eng.	English
2025-2026	Computer Architecture	6	Bachelor	Information Eng.	Italian
2024-2025	**Parallel Programming Fundamentals**	3	**Ph.D.**	DIISM Doctoral School	English
2024-2025	Advanced Computer Architecture	9	Master	Information Eng.	English
2024-2025	Computer Architecture	6	Bachelor	Information Eng.	Italian
2023-2024	Advanced Computer Architecture	9	Master	Information Eng.	English
2023-2024	Computer Architecture	6	Bachelor	Information Eng.	Italian
2022-2023	**Parallel Programming Fundamentals**	2	**Ph.D.**	Italian HPC Sum.School	English
2022-2023	Advanced Computer Architecture	9	Master	Information Eng.	English
2022-2023	Computer Architecture	6	Bachelor	Information Eng.	Italian
2021-2022	**Parallel Programming Fundamentals**	3	**Ph.D.**	Smart Computing	English
2021-2022	Advanced Computer Architecture	9	Master	Information Eng.	English
2021-2022	Computer Architecture	6	Bachelor	Information Eng.	Italian
2020-2021	Advanced Computer Architecture	9	Master	Information Eng.	English
2020-2021	Computer Architecture	6	Bachelor	Information Eng.	Italian
2019-2020	Advanced Computer Architecture	9	Master	Information Eng.	English
2019-2020	Computer Architecture	6	Bachelor	Information Eng.	Italian
2018-2019	Advanced Computer Architecture	9	Master	Information Eng.	English
2018-2019	Computer Architecture	6	Bachelor	Information Eng.	Italian
2017-2018	Advanced Computer Architecture	9	Master	Information Eng.	English
2017-2018	Computer Architecture	6	Bachelor	Information Eng.	Italian

[1] One ECTS credit corresponds to about 8(master)-10(bachelor) hours of teaching and 15-17 additional hours of personal study of the student.

2016-2017	Advanced Computer Architecture	9	Master	Information Eng.	English
2016-2017	Computer Architecture	6	Bachelor	Information Eng.	Italian
2015-2016	Advanced Computer Architecture	9	Master	Information Eng.	English
2015-2016	Computer Architecture	6	Bachelor	Information Eng.	Italian
2014-2015	Advanced Computer Architecture	9	Master	Information Eng.	English
2013-2014	Advanced Computer Architecture	9	Master	Information Eng.	English
2013-2014	Computer Architecture	6	Bachelor	Information Eng.	Italian
2012-2013	Advanced Computer Architecture	9	Master	Information Eng.	English
2012-2013	Computer Architecture	6	Bachelor	Information Eng.	Italian
2011-2012	Advanced Computer Architecture	9	Master	Information Eng.	Italian
2011-2012	Computer Architecture	6	Bachelor	Information Eng.	Italian
2010-2011	Advanced Computer Architecture	9	Master	Information Eng.	Italian
2010-2011	Computer Architecture	6	Bachelor	Information Eng.	Italian
2009-2010	Advanced Computer Architecture	6	Master	Information Eng.	Italian
2009-2010	Computer Architecture	6	Bachelor	Information Eng.	Italian
2008-2009	Advanced Computer Architecture	6	Master	Information Eng.	Italian
2008-2009	Computer Architecture	6	Bachelor	Information Eng.	Italian
2007-2008	**Low Power Architectures**	2	**Ph.D.**	Information Eng.	Italian
2007-2008	Advanced Computer Architecture	6	Master	Information Eng.	Italian
2007-2008	Information Security	3	Master	Manag. of Financial Inst.	Italian
2007-2008	Computer Architecture	6	Bachelor	Information Eng.	Italian
2006-2007	**Low Power Architectures**	2	**Ph.D.**	Information Eng.	Italian
2006-2007	Advanced Computer Architecture	6	Master	Information Eng.	Italian
2006-2007	Information Security	3	Master	Manag. of Financial Inst.	Italian
2006-2007	Computer Architecture	6	Bachelor	Information Eng.	Italian
2005-2006	Advanced Computer Architecture	6	Master	Information Eng.	Italian
2005-2006	Information Security	3	Master	Manag. of Financial Inst.	Italian
2005-2006	Computer Architecture	6	Bachelor	Information Eng.	Italian

As Assistant Professor:

Year	Course	ECTS credits	Level	School	Lang.
2004-2005	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2004-2005	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2004-2005	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2003-2004	C++ Programming Laboratory	2	Master	Information Engineering	Italian
2003-2004	Programming Fundamentals	3	Master	Digital Economy and E-business	Italian
2003-2004	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2003-2004	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2002-2003	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2002-2003	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2002-2003	Programming Fundamentals	3	Master	Digital Economy and E-business	Italian
2002-2003	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2002-2003	Computer Architecture	6	Bachelor	Information Engineering	Italian
2002-2003	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2001-2002	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2001-2002	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2001-2002	Computer Architecture	6	Bachelor	Information Engineering	Italian
2001-2002	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Database management	3	Bachelor	Management of Financial Inst.	Italian
2000-2001	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2000-2001	Database management	3	Master	Management of Financial Inst.	Italian
2000-2001	Computer Architecture	6	Bachelor	Information Engineering	Italian
1999-2000	Advanced Computer Architecture	12	Master	Information Engineering	Italian
1999-2000	Computer Architecture	6	Bachelor	Information Engineering	Italian

International Teaching

Prof. Giorgi held invited lectures on "Multi-Core and Many-Core architectures" at the University of Tampere, Finland in October 2013.

21 Coordination of Teaching and Research Activities

- 2021-present **Scientific Representative of the University of Siena in the RISC-V Foundation**.
- 2021-present **Governing Board Member** of the "CINI - HPC: Key Technologies and Tools" National Lab for High-Performance Computing Key Technologies and Tools.
- 2021-present **Governing Board Member** of the "CINI - Embedded Systems and Smart Manufacturing" National Lab for Embedded Systems and Smart Manufacturing.
- 2018-present **Director of the UNISI Research Unit** of the "CINI" coordinating activities of the local node and re-elected for the second term.
- 2024-2025 **Scientific Coordinator** of the ICSC "EDGE-ME project" coordinating the activities.
- 2024-2025 **Scientific Coordinator** of the Quest-IT "BS5 project" coordinating the activities.
- 2022-2024 **Scientific Coordinator** of the Regione Toscana "HIPERAIHL project" coordinating the activities.
- 2015-2018 **Scientific Coordinator** of the EU "AXIOM project" coordinating the activities of more than 40 researchers across Europe.
- 2010-2014 **Scientific Coordinator** of the EU "TERAFLUX project" coordinating the activities of more than 100 researchers across Europe.
- 2010-2014 **Scientific Coordinator** of the EU "TERAFLUX-INCO project" coordinating the activities of EU-USA collaboration.
- 2008-2009 **Scientific Coordinator** of the Fondazione MPS project: Integration of Sign Language for the Deaf in the digital television.
- 2007-2008 **Scientific Coordinator** of the Regione Toscana project: Digital vocabulary of an automated Sign Language System for the Deaf.
- 2008-2008 **Scientific Coordinator** of the HiPEAC research projet: Cache implications of nonblocking thread execution in a multithreaded architecture.
- 2008-2008 **Scientific Coordinator** of the HiPEAC research project: Multithreaded Dataflow Architectures.
- 2006-2006 **Scientific Coordinator** of the HiPEAC research project: Scalable Multicore Architectures.
- 2004-2005 **Scientific Coordinator** of the FIRB (Scalable Multicore Architectures) project: Innovative Architectures for High Performance Processors.
- 2004-2005 **Scientific Coordinator** of the Fondazione MPS project: Study and Realization of a Multimedia System for Translating and Communicating with the Sign Language for the Deaf.
- 2004-2005 **Scientific Coordinator** of the UNISI project Innovative Architectures for Multimedia Applications in Embedded Systems.
- 2015-2018 **WP-Leader** AXIOM-WP7 - Evaluation and Design Space Exploration.
- 2010-2014 **WP-Leader** TERAFLUX-WP7 - Common Simulation and Compilation Platform.
- 2010-2014 **WP-Leader** TERAFLUX-INCO-WP1 - Integration activities between TERAFLUX and UD.
- 2010-2014 **WP-Leader** ERA-WP1 - Common Simulation and Compilation Platform.
- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2007-present **co-responsible** of the "Computer Architecture Lab", with more than 30 workstations, major computing facilities and having equipment and donations from "AMD", "HP-Labs", "Intel", "NVIDIA", "SECO", "ST-Microelectronics", "Xilinx".

22 Citations by Patents

According to IEEExplore, Roberto Giorgi's papers have been cited by the following patents:

1. Dubrulle, Paul; Goubier, Thierry, and Stéphane Louise, "Speculative and iterative execution of delayed data flow graphs." U.S. Patent Application 10,394,729, filed August 27, 2019.
2. Manet, Philippe; Rousseau, Bertrand, "Tile-based processor architecture model for high-efficiency embedded homogeneous multicore platforms", Patent No. 9275002
3. Manet, Philippe; Rousseau, Bertrand, "A TILE-BASED PROCESSOR ARCHITECTURE MODEL FOR HIGH EFFICIENCY EMBEDDED HOMOGNEOUS MULTICORE PLATFORMS", Patent No. EP2531929
4. Manet, Philippe; Rousseau, Bertrand, "A TILE-BASED PROCESSOR ARCHITECTURE MODEL FOR HIGH EFFICIENCY EMBEDDED HOMOGNEOUS MULTICORE PLATFORMS", Patent No. WO2011092323
5. Rowlands, Joseph B., "BRIDGES PERFORMING REMOTE READS AND WRITES AS UNCACHEABLE COHERENT OPERATIONS", Patent No. 7752281
6. Sano, Barton J.; Rowlands, Joseph B.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS USING MIX OF PACKET COHERENT AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS", Patent No. 7424561
7. Sano, Barton J., "SYSTEM HAVING CONFIGURABLE INTERFACES FOR FLEXIBLE SYSTEM CONFIGURATIONS", Patent No. 7394823
8. Rowlands, Joseph B., "SYSTEM HAVING INTERFACES SWITCH AND MEMORY BRIDGE FOR CC NUMA OPERATION", Patent No. 7266587
9. Sano, Barton J.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS INCLUDING PACKET INTERFACES SWITCHES AND PACKET DMA CIRCUITS FOR SPLITTING AND MERGING PACKET STREAMS", Patent No. 7227870
10. Sano, Barton J.; Rowlands, Joseph B.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS USING MIX OF PACKET COHERENT AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS", Patent No. 7206879
11. Rowlands, Joseph B., "SYSTEM HAVING ADDRESS BASED INTRANODE COHERENCY AND DATA BASED INTERNODE COHERENCY", Patent No. 7003631
12. Rowlands, Joseph B., "L2 CACHE MAINTAINING LOCAL OWNERSHIP OF REMOTE COHERENCY BLOCKS", Patent No. 6993631
13. Rowlands, Joseph B.; Keller, James B., "REMOTE LINE DIRECTORY WHICH COVERS SUBSET OF SHAREABLE CC NUMA MEMORY SPACE", Patent No. 6965973
14. Sano, Barton J.; Rowlands, Joseph B.; Keller, James B.; Moll, Laurent R.; Oner, Koray; Gulati, Manu, "SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC", Patent No. 6941406
15. Sano, Barton J.; Oner, Koray; Moll, Laurent R.; Gulati, Manu, "SYSTEM HAVING TWO OR MORE PACKET INTERFACES A SWITCH AND A SHARED PACKET DMA CIRCUIT", Patent No. 6912602
16. Sano, Barton J.; Rowlands, Joseph B.; Keller, James B.; Moll, Laurent R.; Oner, Koray; Gulati, Manu, "SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC", Patent No. 6748479
17. Rowlands, Joseph B., "System with address-based intranode coherency and data-based internode coherency", Patent No. EP1363191
18. Lin, Chi-Hung; Liao, Che-Yu; Chuang, Ching-Hsiang; Tung, Shing-Wu, "Hybrid simulation system and method", Patent No. 8645116
19. Attinella, John Eric, "CREATING A PHYSICAL TRACE FROM A VIRTUAL TRACE", Patent No. 7853928
20. Dageville, Benoit; Muthukrishnan, Sambavi; Zait, Mohamed, "TECHNIQUES FOR DETERMINING EFFECTS ON SYSTEM PERFORMANCE OF A MEMORY MANAGEMENT PARAMETER", Patent No. 7539608
21. Gupta, Vidyabhusan, "SYSTEM AND METHOD FOR DESIGNING AND OPTIMIZING THE MEMORY OF AN EMBEDDED PROCESSING SYSTEM", Patent No. 7412369