



Date of birth 13th March 1964
Marital Status Married – with two daughters
Languages Italian(native), English(fluent)
Address Dept. Ingegneria dell’Informazione e Scienze Matematiche, Via Roma 56 – 53100 Siena, Italy
Phone work: +39-0577-23-5880, skype: robgiorgi
Email work: giorgi@dii.unisi.it, (personal certified-email: robgiorgi@pec.it)
WWW <http://www.dii.unisi.it/~giorgi>

Main Facts

- Roberto Giorgi is an Associate Professor at Dept. of Information Engineering, University of Siena, Italy.
- For one year, he was Research Associate at the University of Alabama in Huntsville, USA.
- He received his PhD in Computer Engineering and his MS in Electronics Engineering, Summa cum Laude both from University of Pisa, Italy.
- He has received the eligibility (Italian National Abilitation) as Full-Professor since 30th March 2018.
- He coordinated the European Project AXIOM (3.9Meuro cost, 2015-2018, 7 partners), about designing and manufacturing the next generation board for Cyber-Physical Systems.
- He coordinated the TERAFLUX project (8.5Meuro cost, 2010-2014, 11 partners) in the area of Future and Emerging Technologies for Teradevice Computing.
- He is member of the HiPEAC Network of Excellence (High Performance Embedded-system Architecture and Compilation) since 2004.
- He was Deputy Steering Committee in the HiPEAC, Application leader in the ERA project (Embedded Reconfigurable Architectures), participated to SARC (Scalable ARCHitectures) and attracted more than 3 Million Euro of Research Funding to the University of Siena in the last decade.
- He took part in ChARM project, developing software for performance evaluation of ARM-processor based embedded systems with cache memory.
- He has been IEEE Judge for the IEEE-CSIDC (Computer Society International Design Competition).
- He led the project "Bluesign Translator", which received a 5th worldwide prize by IEEE and top companies, and received the FORUM-P.A. prize by the Italian Ministry of Technological and Scientific Innovation, as absolute winner in the category of "actions for the social integration of disadvantaged people through ICT".
- He has been selected by the European Commission as an independent expert for evaluating ICT European Projects.
- He is co-author of more than 120 scientific papers.
- His current interests include Computer Architecture themes such as Embedded Systems, Multiprocessors, Memory System Performance, Workload Characterization.
- He is a Lifetime member of ACM and a Senior Member of the IEEE, IEEE Computer Society.

Contents

1 Appointments	
2 Education	13 Technical Reports and Deliverables
3 Awards	14 Intellectual Property
4 Technology Transfer	15 Educational and Research Software
5 Fields of Interest	16 Public Talks
6 Research Projects	17 Supervised Collaborators/Students
7 Journal Papers [statistics]	18 Professional Activities
8 Monography/Books/Proceedings	19 Major Departmental Committees
9 Book Chapters	20 Teaching
10 Papers in Conference Proceedings	21 Coordination of Teaching and Research Activities
11 Papers: Miscellaneous	22 Citations by Patents
12 Posters	

1 Appointments

Associate Professor of Computer Architecture (with tenure) Oct. 2006-present
University of Siena, Dept. of Information Engineering, Siena, Italy

Assistant Professor of Computer Architecture (with tenure) Mar. 1999-Sept. 2006
University of Siena, Dept. of Information Engineering, Siena, Italy

Post-Doctoral Researcher Feb. 1999-Jan. 2000
The University of Alabama in Huntsville, AL, USA

- “Experimental Research for the Evaluation of Multithreaded Architectures” (NSF grant #9805216)
- “Multithreading Systems” (Italian National Research Council (CNR) grant #203.15.9)

Visiting Scholar May 1998
University of Belgrade, Serbia, Yugoslavia

Visiting Scholar Jul. 1997-Aug.1997
University of Texas in Arlington, TX, USA

Visiting Scholar Jul. 1996-Aug.1996
University of Washington, WA, USA

2 Education

PhD in “Information Engineering: Electronics, Informatics, Telecom.” Oct. 1995-Sept. 1998
University of Pisa, Pisa, Italy

“Evaluation of a Coherence Protocol for Eliminating Passive Sharing in Shared-Bus Multithreaded Multiprocessors”
Thesis advisor: Prof. Cosimo Antonio Prete

MEng in “Electronics Engineering” July 1995
University of Pisa, Pisa, Italy

“Performance Evaluation of Multiprocessor Systems, based on Real Traces Analysis”
Thesis advisor: Prof. Cosimo Antonio Prete
Mark: **Summa cum Laude (110/110+Laude)**

High-School Diploma “Scientific Lyceum” July 1983
Viareggio LU, Italy
Mark: **60/60**

3 Awards

- 2006(May) FORUM P.A./CNIPA Award by **Italian Ministry of Innovation and Technologies** for the best action to accessibility of public administration by the disable through the project “BlueSign Translator” (**absolute winner in the category**). Web sites: <http://www.bluesign.it/> e https://it.wikipedia.org/wiki/Blue_Sign.
- 2002(June) IEEE Award (5th worldwide price 2000 USD) for the realization of a “Sign Language Translator” based on Bluetooth Technology for helping the Deaf in a course projects, IEEE Computer Science International Design Competition (CSIDC).
- Best paper awards for works [C74], [C60], [C42], [C2] (see below).
- Outstanding Contribution Award at IEEE MECO 2014 conference.
- ACM Recognition of Service Award for chairing the ACM Computing Frontiers 2017 conference.

4 Technology Transfer

- 2014-2017 Coordinating the EU-funded Research and Innovation Action AXIOM, which realized through partner SECO an FPGA-based Italian-manufactured single computer board.
- 2007-2009 Cooperation Agreement with RAI (RADIOTELEVISIONE ITALIANA) for the implementation of advanced solutions for the integration of automatic translation systems of Sign Language for the Deaf in the television.
- 2003-2008 Cooperation with Italian Association for the Education of the Deaf (AIES, Associazione Italiana Educazione Sordi) to support the study of a multimedial system for communicating in Italian Sign Language (LIS, Lingua Italiana dei Segni).

- 1998(Nov)-1999(Jan) Contract for “Performance Evaluation of Coherence Protocols for Single-Chip Embedded Multiprocessors” at the Department of Information Engineering, University of Pisa.
- 1995(Sep)-1995(Dec) Contract for “Performance Evaluation of Multiprocessor System under Different Software Workload” at the Department of Information Engineering, University of Pisa.
- 1995(Sep)-1995(Oct) Cooperation with VLSI Tech. Inc., San Jose, CA, U.S.A. to support the realization of X/MOTIF Graphical Interface for the commercial software “ChARM - JumpStart 3.0”.

5 Fields of Interest

- **Scalable, Adaptive and Reconfigurable Systems - enhancing High-Performance Computing architectures** Current High-Performance systems (ranging from the Cloud-Computing to the Embedded-HPC) need more localization of the resources and the paradigms of Edge-Computing and Fog-Computing have been proposed in order to provide a form of proxy to several cloud-based services. At the same time, we are entering the Cyber-Physical age, in which both objects and people will become nodes of the same digital network for exchanging information. Therefore, in our imaginary, the general expectation is that “things” or systems will become somewhat smart as people, allowing rapid and close interactions not only system-system, but also human-system, system-human. More scientifically, we expect that such systems will at least react in real-time, have enough computational power for the assigned tasks, consume the least possible energy for such task (energy efficiency), scale up through modularity, allow for an easy programmability across performance scaling and exploit at best existing standards at minimal costs. The whole set of these expectations impose scientific and technological challenges that need to be properly addressed. In this line of research (projects AXIOM and ERA), we aim at researching new software/hardware architectures to meet the above expectations. The technical approach aims at solving fundamental problems to enable easy programmability of multi-core multi-board systems through the open-source OmpSs programming model, leveraging Distributed Shared Memory (DSM) inspired concepts across the modules. The OmpSs will allow accelerating functions through an FPGA (Agility). In particular, to the best of our knowledge, this is the first time that DSM will be effectively demonstrated on an embedded modular system (eXtensibility). Modular scalability will be possible thanks to a fast interconnect that will enrich the module. To this aim, an innovative modular ARM-based board with enhanced capabilities for interfacing with the physical world will be designed and demonstrated in key scenarios such as Smart Video-Surveillance, Smart Living/Home (Domotic) or others [J30], [J29], [J28], [J27], [J25], [J24], [B10], [C69], [C68], [C67], [C66], [C65],[C64],[C63],[C62],[C61],[C60],[C56],[C54],[C53],[C47],[C46],[C38],[C41],[C24].
- **Architectures and Tools for Many-Core systems - towards Big-Data systems** The ever increasing pace of data poses challenges at several levels in the software-hardware architectures. In this line, future Teradevice Systems, i.e. systems with more than 10^{12} transistors in a single package or multi-layer chip, exhibit a large amount of parallelism (e.g., general purpose 1000 cores) has been explored. Current applications and programming models are not yet using this type of systems efficiently. The work done in this field of research regards the development of architectures that both builds on existing solutions at the architectural level and try to enable the execution of parallel programs even in the case of sequential programming models. This is made possible by exploiting a parallel generation and scheduling of threads and combining concepts of dataflow. Big-data can be managed in a vary efficient way using Dataflow Supercomputing [G6], which can rely on Dataflow Engines now available on the market [B3]. An essential aspect becomes to be able to assess the performance of these new platforms that not yet exist, using appropriate tools [J31] [J22],[J21],[J20],[J18],[J17],[J13],[B10],[C59],[C58],[C57],[C55],[C50],[C45],[C49],[C48],[C42]. In addition, applications are becoming more complex, requiring more computational resources as they need to process larger and larger amounts of data (“big-data”); a typical examples are bioinformatics applications as we need a shorter time to analyze biological data and have more precise information on the health status of a patient. Processing may not necessarily be a classic data-parallel problem: in the general case of irregular applications, the effort required the programmer can be very high or even not feasible. For this reason, in this line of research we examine the methodologies that enable a more efficient execution, regardless of what the programmer specifies, by improving the hardware/software interface. The contribution in this area is a proposal for a radical change in the way applications run on the architecture, using however minimal changes to the architecture itself. The proposal is currently focusing on the use of an extended instruction set (“called T-Star”, consisting of only six instructions) and its architectural support. In order to demonstrate the applicability to current computing systems we used the x86.64 architecture, but we analyzed the feasibility also on other previous architectures such as the Cell Processor from Sony-Toshiba-IBM [C36],[C35],[C34],[C33],[C31].
- **Low-Power techniques for Embedded Systems** One of the most critical parts of an embedded system is the cache memory, since it affects performance and large portions of the power consumption. In particular, the losses (leakage) continue to be a problem despite the use of new materials with high dielectric constant (Hi-K) and even in the 11nm technology nodes and at normal operating temperatures (over 30 degrees Celsius). An innovative proposal is based on the filtering effects of a non-low-power cache stage followed by a low-power cache stage. Significant improvements can so be achieved at virtually negligible costs in terms of area and complexity [C37],[C32],[C30],[C29].
- **Design techniques for architectural support of Elliptic Curve Cryptography** The cryptographic systems based on elliptic curves (or ECC Elliptic Curve Cryptography) have the advantage to work with operands of a

length of at least one order of magnitude lower than that of cryptographic standards now commonly in use, such as RSA, DSA, Diffie-Hellman, El-Gamal. Because of this important feature, cryptosystems based on elliptic curves are particularly suitable for use on smart cards and devices like the mobile and embedded applications. Typically, there are two possible solutions to improve the performance of ECC systems: the first is the optimization of the software, the second is the realization in hardware arithmetic coprocessors. The software implementation is certainly flexible, but the performance that would be obtained in the embedded devices are inadequate; on the contrary, hardware processing is expensive and does not offer the desired flexibility. The research carried out, using the instruction set of ARM processors, widely used in embedded applications, show promising results. The architectural support that involves on the one hand the minimum hardware changes has been identified. This has also other benefits in terms of reducing the execution time and the overall used resources [J16],[J14],[J9],[C22],[C20].

- **Evaluation and proposal of a new microprocessor architecture based on multithreading and dataflow concepts, which enables to overcome traditional limitations of Superscalars and VLIWs** In this research line, it has been analyzed the possibility of using a new processor architecture that could improve considerably the performance of current architectures based mainly on the Superscalar and VLIW paradigms. This research has led to the definition of a new type of microprocessor that builds on the concepts of dataflow and expresses them fully in current multithreaded systems. The architecture is named Scheduled Data-Flow (SDF) and it has been expanded into novel models called Decoupled Threaded Architecture (DTA). Later developments led to the TERAFLUX architecture. Several generations of simulators have been developed in order to arrive lately to model a full-system 'as-is' running an off-the-shelf Linux Operating System and consisting of multiple cores (up to 32 per node have been explored) and multiple nodes. The results were very encouraging already with the first simulated prototypes and demonstrates that this type of architecture allows not only to achieve superior performance in respect to current superscalar processors and VLIWs, but also to fully exploit the thread-level parallelism, thus overcoming the limitations of scalability of the processor internal resources (e.g., limited instruction level parallelism) of current architectures [J29], [J26], [J22], [J21], [G6], [B9], [B8], [B7], [B6],[B5],[B4],[B3],[J19],[J17],[J8],[J7],[J6],[J5],[C59],[C51],[C44],[C43],[C40],[C39],[C28],[C17],[C12].
- **Innovative solutions for cache-coherence of single-chip multiprocessor systems under thread migration** In this line of research, it has been proposed a new coherence protocol, called PSCR (Shared Passive Copy Removal), evaluated in the case of shared-bus, shared-memory multicores. This architecture is particularly attractive given its low cost and simplicity and in fact it has been adopted since the year 2000 by all major processor manufacturers. While it is necessary to introduce private cache memories in order to overcome the limitations of an excessive traffic on the shared-bus, we also need to introduce mechanisms to manage the consistency of multiple copies of the application data. This problem is exacerbated by thread migration to available cores, in turn necessary to balance the load in the machine. However, this research highlighted that a considerable part of the traffic is unnecessary because it is due to copies that mistakenly appear as shared while they are actually private: this situation has been named "passive sharing". The proposed solution consist in a novel coherence protocol (PSCR) that completely eliminate the passive sharing. The evaluation of such protocol demonstrated that PSCR can achieve a higher scalability as compared to six other protocols known in the literature or widely used, such as the MESI protocol. The results showed that with the use of PSCR, multicores with more than 30 cores are feasible even with a simple and inexpensive solution such as the shared-bus interconnect [J3],[J2],[J1],[C10],[C7],[C4],[C3],[C2],[C1].
- **Study of solutions for improving performance of Web-Servers and Data-Base Management Systems (DBMS)** Web servers and DBMSs (Data Base Management Systems) are particularly critical from the point of view of performance. E.g., E-Commerce systems, OLTP systems (Online Transaction Processing) and DSSs (Decision Support System) are implemented with an N-tier distributed architecture or also simply with a three-tier architecture, in which second layer acts primarily a Web-Server and third layer acts primarily a DBMS (being the first layer consists of the client or Web browser). To cope with a high number of requests, the typical solution is to use a Network of Workstations (or Clusters). In cases where the single node constitutes a multicore system, it is necessary to use every possible solution to maximize performance. In particular, taking into account the organization of the system, the machine load (workload) consists of intense multitasking activity (generated by both Web client requests and DB queries) that involves a strong commitment Operating System (e.g., Scheduler, Virtual Memory) in order to obtain a balanced load. Taking this platform as a case study, we tried to highlight possible architectural solutions to improve significantly the performance of the machine. Through the combined intervention on restructuring of kernel data, operating system virtual mapping, OS scheduler and the coherence protocol, we found out that it is possible even to double the performance of a multicore system. The evaluation methodology is based on widespread benchmarks such as TPC-W and TPC-D [J12],[J11],[J10],[C21],[C19],[C16],[C15],[C14],[C13],[C11],[C9].
- **Handheld Multimedia Devices for the Deaf** Starting from the analysis of the actual needs of the Deaf, it emerged that the Deaf prefers to communicate through the sign language, because it is perceived as their mother tongue and, in fact, it allows an immediacy of communication otherwise difficult to obtain. The current developments in information technology and the increase of the processing power of portable devices (in particular smart-phones, handheld computers and other mobile devices) enabled to think about the design of assistive technology that can make an automatic translation of text into sign language for the Deaf. As the processing power and energy consumption of portable devices are anyway limited, appropriate solutions have to be explored in order to enable an acceptable usability by the Deaf Community. This research achieved a working prototype that is able to translate natural language text (in this study, Italian) into Italian Sign Language (LIS). Moreover, a digital dictionary has

been constructed and validated with the help of the Deaf. This dictionary extends the current state-of-the art paper dictionary by more than 20% of terms [J15],[C27],[C26],[C25],[C23].

- **Innovative cache design techniques for designing embedded systems and for computer architecture education** The processing system internals contain many details which cannot be checked directly, such the importance of pipelines or caches. Therefore, it is crucial to rely on experimental tools capable on the one hand to understand the inside of the microprocessor and the cache memory through a simple web-based interface and on the other hand to enable the teacher to monitor the student activities while he/she is exploring the complexity of the processor. In this research, new tools had been implemented. Interestingly, some of the features of those tools (such as the exploration of 3D locality curves) has been found useful also for system designer and has been included in commercial tools such as the ChARM for the VLSI Technology Inc. Jumpstart Kit [J4],[C52],[C18],[C8],[C6][C5].

6 Research Projects

- R20. 2015-2018 Role: **Coordinator(PI)** (European Commission - H2020), “**AXIOM: Agile, eXtensible, fast I/O Module for the cyber-physical era**” - project id. 645496, (EUR 3’945’937 total funding, EUR **985’000** for UNISI) - Selection Mark: 14.5/15.
- R19. 2015-2018 Role: **Workpackage Leader WP7 “Evaluation and Design Space Exploration”** (European Commission - H2020), “**AXIOM: Agile, eXtensible, fast I/O Module for the cyber-physical era**” - project id. 645496.
- R18. 2012-2014 Role: **Coordinator(PI)** (European Commission - Special FP7-FET objective for cooperating with non-EU partners), Future and Emerging Technologies - Large Project - TERAFLUX–INCO “Exploiting Dataflow Parallelism in Teradevice Computing in cooperation with University of Delaware, USA” - project id. 309229, (EUR 420’000 total funding, EUR **150’000** for UNISI) - Selection Mark: 15/15.
- R17. 2010-2014 Role: **Workpackage Leader WP1 “Integration activities between TERAFLUX and UD”** (European Commission - FP7-FET), Future and Emerging Technologies - Large Project - “TERAFLUX – Exploiting Dataflow Parallelism in Teradevice Computing in cooperation with University of Delaware, USA” - project id. 309229.
- R16. 2010-2014 Role: **Coordinator(PI)** (European Commission - FP7-FET), TERAFLUX: “Exploiting Dataflow Parallelism in Teradevice Computing” project id. 249013, (EUR 5’700’000 total funding, EUR **1’167’000** for UNISI) - Selection Mark: 15/15.
- R15. 2010-2014 Role: **Workpackage Leader WP7 “Common Simulation and Compilation Platform”** (European Commission - FP7-FET), “TERAFLUX – Exploiting Dataflow Parallelism in Teradevice Computing” project id. 249013.
- R14. 2010-2013 Role: **Workpackage Leader WP1 “Embedded Application Analysis”** (European Commission - FP7-ICT), ERA: “Embedded Reconfigurable Architecture” - project id. 249059, (EUR 2’800’000 total funding, EUR **417’000** for UNISI).
- R13. 2010-2014 Role: **Participation** (HiPEAC networking funding), **HIPEAC3: “High-Performance Embedded Architecture and Compilation”**, (EUR 4’000 total funding, EUR **4’000** for UNISI).
- R12. 2008-2009 Role: **Coordinator(PI)** (Monte dei Paschi di Siena Foundation), “Integration of Sign Language for the Deaf in the digital television”, (EUR 50’000 total funding, EUR **50’000** for UNISI).
- R11. 2007-2008 Role: **Coordinator(PI)** (Regione Toscana - through National Association of the Deaf), “Extension of the digital vocabulary of an automated Sign Language System for the Deaf”, (EUR 10’000 total funding, EUR **10’000** for UNISI).
- R10. 2008-2012 Role: **Participation** (HiPEAC networking funding), HiPEAC Network of Excellence **HIPEAC2: “High-Performance Embedded Architecture and Compilation”**, (EUR 5’000 total funding, EUR **5’000** for UNISI).
- R9. 2008 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), HiPEAC Network of Excellence “**Multithreaded Dataflow Architectures**”, (EUR 10’240 total funding, EUR **10’240** for UNISI).
- R8. 2008 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), “**Cache implications of non-blocking thread execution in a multithreaded architecture**”, (EUR 14’000 total funding, EUR **14’000** for UNISI).
- R7. 2005-2009 Role: **Participation** (European Commission - FP6-FET), Future and Emerging Technologies - Integrated Project (IP) SCALA/SARC: “Scalable ARChitectures”, (EUR 8’500’000 total funding, EUR **(through University of Pisa) 90’000** for UNISI).
- R6. 2006 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), HiPEAC Network of Excellence “Scalable Multicore Architectures” in Cooperation with Universities of Goteborg-Chalmers (Sweden), Delft-TUD (Netherlands), Barcelona-UPC (Spain), (EUR 30’000 total funding, EUR **10’000** for UNISI).

- R5. 2004-2008 Role: **Deputy Steering Committee** (European Commission - FP6-NoE), [HiPEAC Network of Excellence “High-Performance Embedded Architecture and Compilation”](#), coordination: Polytechnic University of Catalonia, Spain (UPC), (EUR 3’900’000 total funding, EUR **n/a** for UNISI).
- R4. 2004-2005 Role: **Coordinator(PI)** (Italian Investment Fund for Basic Research (FIRB), Italian Ministry of Education, University and Research (MIUR)), “Innovative Architectures for High Performance Processors”, (EUR 60’000 total funding, EUR **30’000** for UNISI).
- R3. 2004 Role: **Coordinator(PI)** (Monte dei Paschi di Siena Foundation), “Study and Realization of a Multimedia System for Translating and Communicating with the Sign Language for the Deaf”, (EUR 40’000 total funding, EUR **40’000** for UNISI).
- R2. 2004-2005 Role: **Coordinator(PI)** (University Research Plan (PAR) of the University of Siena), “Innovative Architectures for Multimedia Applications in Embedded Systems”, (EUR 15’000 total funding, EUR **15’000** for UNISI).
- R1. 2003-2005 Role: **Participation** (Italian Investment Fund for Basic Research (FIRB), Italian Ministry of Education, University and Research (MIUR)), “Reconfigurable Platforms for Broadband Mobile Devices”, activity of “Development of Innovative Cryptographic Techniques”, coordinator prof. Enrico Martinelli, (EUR 320’000 total funding, EUR **80’000** for UNISI).

7 Journal Papers [\[statistics\]](#)

- J33. A. Filgueras, M. Vidal, M. Mateu, D. Jiménez-González, C. Álvarez, X. Martorell, E. Ayguadé, D. Theodoropoulos, D. Pnevmatikatos, P. Gai, S. Garzarella, D. Oro, J. Hernando, N. Bettin, A. Pomella, M. Procaccini, R. Giorgi, “[The AXIOM Project: IoT on Heterogeneous Embedded Platforms](#)”, *IEEE Design and Test*, vol. pre-print, Nov. 2019, pp. 1-6, ISSN: 2168-2356, SCOPUS: 2-s2.0-85074820785, DOI: [10.1109/MDAT.2019.2952335](#).
- J32. R. Giorgi, F. Khalili, M. Procaccini, “[Translating Timing into an Architecture: the Synergy of COTSon and HLS \(Domain Expertise: Designing a Computer Architecture via HLS\)](#)”, *Int.l Journal of Reconfigurable Computing*, London, UK, 2 Sept.2 2019, pp. 1-18, ISSN: 1687-7209, SCOPUS: 2-s2.0-85075350510, DOI: [10.1155/2019/2624938](#).
- J31. R. Giorgi, “Scalable Embedded Computing through Reconfigurable Hardware: comparing DF-Threads, Cilk, OpenMPI and Jump”, *ELSEVIER Microprocessors and Microsystems*, vol. 63, Aug. 2018, pp. 66-74, ISSN: 0141-9331, SCOPUS: 2-s2.0-85053430111, DOI: [10.1016/j.micpro.2018.08.005](#).
- J30. D. Theodoropoulos, S. Mazumdar, E. Ayguade, N. Bettin, J. Bueno, S. Ermini, A. Filgueras, D. Jimenez-Gonzalez, C. Alvarez Martinez, X. Martorell, F. Montefoschi, D. Oro, D. Pnevmatikatos, A. Rizzo, P. Gai, S. Garzarella, B. Morelli, A. Pomella, R. Giorgi, “The AXIOM platform for next-generation cyber physical systems”, *ELSEVIER Microprocessors and Microsystems*, 2017, pp. 540-555, ISSN: 0141-9331, SCOPUS: 2-s2.0-85021936895, WOS:000407984000049, DOI: [10.1016/j.micpro.2017.05.018](#).
- J29. L. Verdoscia, R. Giorgi, “A Data-Flow Soft-Core Processor for Accelerating Scientific Calculation on FPGAs”, *Mathematical Problems in Engineering*, vol. 2016, no. 1, Apr. 2016, pp. 1-21, (article ID 3190234), ISSN: 1563-5147, SCOPUS: 2-s2.0-84973355670, DOI: [10.1155/2016/3190234](#).
- J28. A. Rizzo, G. Burrelli, F. Montefoschi, M. Caporali, R. Giorgi, “[Making IoT with UDOO](#)”, *Interaction Design and Architecture(s)*, vol. 1, no. 30, Dec. 2016, pp. 95-112, ISSN: 1826-9745, SCOPUS: 2-s2.0-85007362581, WOS:000393571700007.
- J27. C. Alvarez, E. Ayguade, J. Bosch, J. Bueno, A. Cherkashin, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, N. Navarro, M. Vidal, D. Theodoropoulos, D. Pnevmatikatos, D. Catani, D. Oro, C. Fernandez, C. Segura, J. Rodriguez, J. Hernando, C. Scordino, P. Gai, P. Passera, A. Pomella, N. Bettin, A. Rizzo, R. Giorgi, “The AXIOM Software Layers”, *ELSEVIER Microprocessors and Microsystems*, vol. 47, Part B, 2016, pp. 262-277, ISSN: 0141-9331, SCOPUS: 2-s2.0-84979544372, WOS:000390513300003, DOI: [10.1016/j.micpro.2016.07.002](#).
- J26. S. Weis, A. Garbade, B. Fechner, A. Mendelson, R. Giorgi, T. Ungerer, “[Architectural Support for Fault Tolerance in a Teradevice Dataflow System](#)”, *Springer Int.l Journal of Parallel Programming*, New York, NY, USA, vol. 44, no. 2, Apr 2016, pp. 208-232, ISSN: 1573-7640, SCOPUS: 2-s2.0-84901582160, WOS:000373569600002, DOI: [10.1007/s10766-014-0312-y](#).
- J25. R. Giorgi, S. Mazumdar, S. Viola, P. Gai, S. Garzarella, B. Morelli, D. Pnevmatikatos, D. Theodoropoulos, C. Alvarez, E. Ayguade, J. Bueno, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, “Modeling Multi-Board Communication in the AXIOM Cyber-Physical System”, *Ada User Journal*, vol. 37, no. 4, December 2016, pp. 228-235, ISSN: 1381-6551, SCOPUS: 2-s2.0-85004143304.
- J24. P. Burgio, C. Alvarez, E. Ayguade, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, N. Navarro, R. Giorgi, “Simulating next-generation cyber-physical computing platforms”, *Ada User Journal*, vol. 37, no. 1, Mar. 2016, pp. 59-63, ISSN: 1381-6551, SCOPUS: 2-s2.0-84974555745.

- J23. S. Wesner, L. Schubert, R. Badia, A. Rubio, P. Paolucci, R. Giorgi, “Special Section on Terascale Computing”, *ELSEVIER Future Generation Computer Systems*, New York, NY, USA, vol. 53, July 2015, pp. 88-89, SCOPUS: 2-s2.0-84939190506, WOS:000361075400008, DOI: [10.1016/j.future.2015.07.015](https://doi.org/10.1016/j.future.2015.07.015).
- J22. R. Giorgi, A. Scionti, “A scalable thread scheduling co-processor based on data-flow principles”, *ELSEVIER Future Generation Computer Systems*, Amsterdam, Netherlands, vol. 53, Dec. 2015, pp. 100-108, ISSN: 0167-739X, SCOPUS: 2-s2.0-84939202928, WOS:000361075400010, DOI: [10.1016/j.future.2014.12.014](https://doi.org/10.1016/j.future.2014.12.014).
- J21. R. Giorgi, “Transactional Memory on a Dataflow Architecture for Accelerating Haskell”, *WSEAS Trans. Computers*, vol. 14, 2015, pp. 546-558, ISSN: 1109-2750.
- J20. P. Burgio, C. Alvarez, E. Ayguadé, A. Filgueras, D. Jiménez-González, X. Martorell, N. Navarro, R. Giorgi, “Simulating next-generation Cyber-physical computing platforms”, *Ada User Journal*, vol. 36, no. 4, Dec. 2015, pp. 259-263, ISSN: 1381-6551, SCOPUS: 2-s2.0-84960085502.
- J19. R. Giorgi, R. Badia, F. Bodin, A. Cohen, P. Evripidou, P. Faraboschi, B. Fechner, G. Gao, A. Garbade, R. Gayatri, S. Girbal, D. Goodman, B. Khan, S. Koliai, J. Landwehr, N. Minh, F. Li, M. Luján, A. Mendelson, L. Morin, N. Navarro, T. Patejko, A. Pop, P. Trancoso, T. Ungerer, I. Watson, S. Weis, S. Zuckerman, M. Valero, “TERAFLUX: Harnessing dataflow in next generation teradevices”, *ELSEVIER Microprocessors and Microsystems*, Netherlands, Amsterdam, vol. 38, no. 8, Part B, 2014, pp. 976-990, ISBN: N/A, ISSN: 0141-9331, SCOPUS: 2-s2.0-84912558447, WOS:000347755500013, DOI: [10.1016/j.micpro.2014.04.001](https://doi.org/10.1016/j.micpro.2014.04.001).
- J18. A. Portero, Z. Yu, R. Giorgi, “TERAFLUX: Exploiting Tera-device Computing Challenges”, *ELSEVIER Procedia Computer Science*, New York, NY, USA, vol. 7, 2011, pp. 146-147, (Proc. 2nd European Future Technologies Conf. and Exhibition 2011 (FET 11)), ISBN: N/A, ISSN: 1877-0509, SCOPUS: 2-s2.0-84856501660, WOS:000299100900045, DOI: [10.1016/j.procs.2011.09.081](https://doi.org/10.1016/j.procs.2011.09.081).
- J17. S. Bartolini, I. Branovic, R. Giorgi, E. Martinelli, “Effects of Instruction-set Extensions on an Embedded Processor: a Case Study on Elliptic Curve Cryptography over GF(2^{sup m})”, *IEEE Trans. Computers*, Los Alamitos, CA, USA, vol. 57, no. 5, May 2008, pp. 672-685, ISBN: N/A, ISSN: 0018-9340, SCOPUS: 2-s2.0-64349109200, WOS:000254054500008, DOI: [10.1109/TC.2007.70832](https://doi.org/10.1109/TC.2007.70832).
- J16. S. Bartolini, P. Bennati, R. Giorgi, “L’Informatica per i sordi: su palmare la lingua dei segni”, *Mondo Digitale*, June 2007, pp. 42-49, ISSN: 1720898X, SCOPUS: 2-s2.0-34547978230.
- J15. S. Bartolini, P. Foglia, R. Giorgi, C. Prete, “MEemory performance: DEaling with Applications, systems and architecture”, *ACM SIGARCH Computer Architecture News*, New York, NY, USA, vol. 34, no. 1, Mar. 2006, pp. 1-2, ISSN: 0163-5964, SCOPUS: 2-s2.0-36749070946, DOI: [10.1145/1152779.1147352](https://doi.org/10.1145/1152779.1147352).
- J14. S. Bartolini, R. Giorgi, “Issues in Embedded Single-Chip Multicore Architectures”, *Journal of Embedded Computing*, Amsterdam, Netherlands, vol. 2, no. 2, Dec. 2006, pp. 137-139, ISSN: 1740-4460.
- J13. P. Foglia, R. Giorgi, C. Prete, “Reducing coherence overhead and boosting performance of high-end SMP multiprocessors running a DSS workload”, *ELSEVIER Journal of Parallel and Distributed Computing*, Amsterdam, Netherlands, vol. 65, no. 3, Mar. 2005, pp. 289-306, ISBN: N/A, ISSN: 0743-7315, SCOPUS: 2-s2.0-14544307829, WOS:000227568200004, DOI: [10.1016/j.jpdc.2004.10.003](https://doi.org/10.1016/j.jpdc.2004.10.003).
- J12. S. Bartolini, P. Foglia, R. Giorgi, C. Prete, “Memory Performance: Dealing with Applications, Systems and Architecture”, *SIGARCH Comput. Archit. News*, New York, NY, vol. 34, no. 1, Sept. 2005, pp. 2, ISSN: 0163-5964, SCOPUS: 2-s2.0-85027395178, DOI: [10.1145/1147349.1147352](https://doi.org/10.1145/1147349.1147352).
- J11. P. Foglia, R. Giorgi, C. Prete, “Speeding-up multiprocessors running DBMS workloads through coherence protocol”, *Int. J. High Performance Computing and Networking*, Olney, Bucks. (UK), vol. 1, no. 1/2, June 2004, pp. 17-32, ISSN: 1740-0562, SCOPUS: 2-s2.0-58149302977, DOI: [10.1504/IJHPCN.2004.007562](https://doi.org/10.1504/IJHPCN.2004.007562).
- J10. P. Foglia, R. Giorgi, C. Prete, “Simulation Study of Memory Performance of SMP Multiprocessors Running a TPC-W Workload”, *IEE Proceedings Computers and Digital Techniques*, London, UK, vol. 151, no. 2, Mar. 2004, pp. 93-109, ISBN: N/A, ISSN: 1350-2387, SCOPUS: 2-s2.0-1642295014, WOS:000220430400001, DOI: [10.1049/ip-cdt:20040349](https://doi.org/10.1049/ip-cdt:20040349).
- J9. I. Branovic, R. Giorgi, E. Martinelli, “A Workload Characterization of Elliptic Curve Cryptography Methods in Embedded Environments”, *ACM SIGARCH Computer Architecture News*, New York, NY, USA, vol. 32, no. 3, June 2004, pp. 27-34, ISSN: 0163-5964, SCOPUS: 2-s2.0-77953567600, DOI: [10.1145/1024295.1024299](https://doi.org/10.1145/1024295.1024299).
- J8. K. Kavi, R. Giorgi, J. Arul, “Scheduled Dataflow: Execution Paradigm, Architecture, and Performance Evaluation”, *IEEE Trans. Computers*, Los Alamitos, CA, USA, vol. 50, no. 8, Aug. 2001, pp. 834-846, ISBN: N/A, ISSN: 0018-9340, SCOPUS: 2-s2.0-0035416089, WOS:000170643500007, DOI: [10.1109/12.947011](https://doi.org/10.1109/12.947011).
- J7. R. Giorgi, “Memory Decoupled Architectures and related issues Guest Editor’s Introduction”, *IEEE TCCA Newsletter*, Los Alamitos, CA, USA, Jan. 2001, pp. 2-4, ISSN: 1041-1186 .

- J6. S. Bartolini, R. Giorgi, J. Protic, C. Prete, M. Valero, “Parallel Architecture and Compilation Techniques: Selection of workshop papers, Guests’ Editors Introduction”, *ACM SIGARCH Computer Architecture News*, New York, NY, USA, vol. 29, no. 5, Dec. 2001, pp. 9-12, ISSN: 0163-5964, DOI: [10.1145/563647.563651](https://doi.org/10.1145/563647.563651).
- J5. K. Kavi, J. Arul, R. Giorgi, “Execution and Cache Performance of the Scheduled Dataflow Architecture”, *SPRINGER Journal of Universal Computer Science*, New York, NY, (USA), vol. 6, no. 10, Oct. 2000, pp. 948-967, **Special Issue on Multithreaded Processors and Chip Multiprocessors**, ISSN: 0948-6968, SCOPUS: 2-s2.0-0000254845, DOI: [10.3217/jucs-006-10-0948](https://doi.org/10.3217/jucs-006-10-0948).
- J4. R. Giorgi, C. Prete, “An Educational Environment for Designing and Performance Tuning of Embedded Systems”, *IEEE TCCA Newsletter*, Los Alamitos, CA, USA, Feb. 1999, pp. 54-56, ISSN: 1041-1186 .
- J3. R. Giorgi, C. Prete, “PSCR: A Coherence Protocol for Eliminating Passive Sharing in Shared-Bus Shared-Memory Multiprocessors”, *IEEE Trans. Parallel and Distributed Systems*, Vol. 10, No. 7, Los Alamitos, CA, USA, July 1999, pp. 742-763, ISBN: N/A, ISSN: 1045-9219, SCOPUS: 2-s2.0-0033363130, WOS:000081713100006, DOI: [10.1109/71.780868](https://doi.org/10.1109/71.780868).
- J2. C. Prete, G. Prina, R. Giorgi, L. Ricciardi, “Some Considerations About Passive Sharing in Shared-Memory Multiprocessors”, *IEEE TCCA Newsletter*, Los Alamitos, CA, USA, Mar. 1997, pp. 34-40, ISSN: 1041-1186.
- J1. R. Giorgi, C. Prete, G. Prina, L. Ricciardi, “Trace Factory: Generating Workloads for Trace-Driven Simulation of Shared-Bus Multiprocessors”, *IEEE Concurrency*, Los Alamitos, CA, USA, vol. 5, no. 4, Oct. 1997, pp. 54-68, ISBN: 0-8186-7743-0, ISSN: 1092-3063, SCOPUS: 2-s2.0-0031246107, WOS:A1997YH98400010, DOI: [10.1109/4434.641627](https://doi.org/10.1109/4434.641627).

8 Monography/Books/Proceedings

- G6. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “Guide to DataFlow Supercomputing”, *Springer*, Berlin, DE, Apr 2015, pp. 1-127, ISBN: 978-3-319-16228-7, ISSN: 1617-7975, WOS:000374480500008, DOI: [10.1007/978-3-319-16229-4](https://doi.org/10.1007/978-3-319-16229-4).
- G5. R. Giorgi, S. Wong, “WRC’10: Proc. 2010 Workshop on Reconfigurable Computing”, *TU-Delft / EWI Computer Engineering Laboratory*, Delft, The Netherlands, Jan. 2010, pp. 1-116, ISBN: 978-90-72298-05-8.
- G4. S. Bartolini, P. Foglia, R. Giorgi, C. Prete, “MEDEA ’09: Proc. 2009 workshop on MEmory performance”, *ACM*, New York, NY, USA, Sept. 2009, pp. 1-48, ISBN: 978-1-60558-830-8, SCOPUS: 2-s2.0-74749100609, DOI: [10.1145/1621960](https://doi.org/10.1145/1621960).
- G3. S. Bartolini, P. Foglia, R. Giorgi, C. Prete, “MEDEA ’08: Proc. 2008 workshop on MEmory performance”, *ACM*, New York, NY, USA, Oct. 2008, pp. 1-84, ISBN: 978-1-60558-243-6, SCOPUS: 2-s2.0-77954464017, DOI: [10.1145/1509084](https://doi.org/10.1145/1509084).
- G2. S. Bartolini, P. Foglia, R. Giorgi, C. Prete, “MEDEA ’07: Proc. 2007 workshop on MEmory performance”, *ACM*, New York, NY, USA, 2007, pp. 1-113, ISBN: 978-1-59593-807-7, SCOPUS: 2-s2.0-77954506101, DOI: [10.1145/1327171](https://doi.org/10.1145/1327171).
- G1. S. Bartolini, P. Foglia, R. Giorgi, C. Prete, “Proc. 2006 workshop on MEmory performance: DEaling with Applications, systems and architectures”, *ACM Press*, New York, NY, U.S.A., 2006, pp. 1-52, ISBN: 1-59593-568-1, DOI: [10.1145/1166133](https://doi.org/10.1145/1166133).

9 Book Chapters

- B11. R. Giorgi, “Exploring Future Many-Core Architectures: The TERAFLUX Evaluation Framework”, *Elsevier*, 2017, pp. 33-72, ISSN: 0065-2458, SCOPUS: 2-s2.0-85008936555, WOS:000403245600003, DOI: [10.1016/bs.adcom.2016.09.002](https://doi.org/10.1016/bs.adcom.2016.09.002).
- B10. R. Giorgi, N. Bettin, P. Gai, X. Martorell, A. Rizzo, “AXIOM: A Flexible Platform for the Smart Home”, *Springer Int.l Pub.*, Cham, 2016, pp. 57-74, ISBN: 978-3-319-42304-3, SCOPUS: 2-s2.0-85006445773, DOI: [10.1007/978-3-319-42304-3.3](https://doi.org/10.1007/978-3-319-42304-3.3).
- B9. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “Guide to DataFlow Supercomputing Basic Concepts, Case Studies, and a Detailed Example Postscript”, *Springer*, Berlin, DE, Apr 2015, pp. 125-125, ISBN: 978-3-319-16228-7, ISSN: 1617-7975, WOS:000374480500007, DOI: [10.1007/978-3-319-16229-4](https://doi.org/10.1007/978-3-319-16229-4).
- B8. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “Guide to DataFlow Supercomputing Basic Concepts, Case Studies, and a Detailed Example Epilogue”, *Springer*, Berlin, DE, Apr 2015, pp. 123-123, ISBN: 978-3-319-16228-7, ISSN: 1617-7975, WOS:000374480500006, DOI: [10.1007/978-3-319-16229-4](https://doi.org/10.1007/978-3-319-16229-4).
- B7. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “Guide to DataFlow Supercomputing Basic Concepts, Case Studies, and a Detailed Example Preface”, *Springer*, Berlin, DE, Apr 2015, pp. V-V, ISBN: 978-3-319-16228-7, ISSN: 1617-7975, WOS:000374480500001, DOI: [10.1007/978-3-319-16229-4](https://doi.org/10.1007/978-3-319-16229-4).
- B6. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “Using the WebIDE”, *Springer Int.l Publishing*, 2015, pp. 107-122, ISBN: 9783319162294, ISSN: 1617-7975, WOS:000374480500005, DOI: [10.1007/978-3-319-16229-4.4](https://doi.org/10.1007/978-3-319-16229-4.4).

- B5. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “An Example Application: Fourier Transform”, *Springer Int.l Publishing*, 2015, pp. 73-106, ISBN: 9783319162294, ISSN: 1617-7975, WOS:000374480500004, DOI: [10.1007/978-3-319-16229-4_3](https://doi.org/10.1007/978-3-319-16229-4_3).
- B4. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “Selected Case Studies”, *Springer Int.l Publishing*, 2015, pp. 41-72, ISBN: 9783319162294, ISSN: 1617-7975, WOS:000374480500003, DOI: [10.1007/978-3-319-16229-4_2](https://doi.org/10.1007/978-3-319-16229-4_2).
- B3. V. Milutinovic, J. Salom, N. Trifunovic, R. Giorgi, “The DataFlow Paradigm”, *Springer Int.l Publishing*, 2015, pp. 1-39, ISBN: 9783319162294, ISSN: 1617-7975, WOS:000374480500002, DOI: [10.1007/978-3-319-16229-4_1](https://doi.org/10.1007/978-3-319-16229-4_1).
- B2. S. Wong, L. Carro, M. Rutzig, D. Matos, R. Giorgi, N. Puzovic, S. Kaxiras, M. Cintra, G. Desoli, P. Gai, S. Mckee, A. Zaks, “**ERA—Embedded Reconfigurable Architectures**”, *Springer New York*, Aug 2011, pp. 239-259, ISBN: 978-1-4614-0061-5, ISSN: N/A, WOS:000294271300010, DOI: [10.1007/978-1-4614-0061-5i_10](https://doi.org/10.1007/978-1-4614-0061-5i_10).
- B1. S. Bartolini, R. Giorgi, E. Martinelli, “Instruction Set Extensions for Cryptographic Applications”, *Springer*, 2009, pp. 191-233, ISBN: 978-0-387-71816-3, DOI: [10.1007/978-0-387-71817-0_9](https://doi.org/10.1007/978-0-387-71817-0_9).

10 Papers in Conference Proceedings

- C74. L. Verdoscia, A. Sahebi, R. Giorgi, “A Data-Flow Methodology for Accelerating FFT”, *IEEE 8th Mediterranean Conf. on Embedded Computing (MECO)*, June 2019, pp. 471-474, **Best Paper Award**, ISBN: 978-1-7281-1740-9, ISSN: 2377-5475, SCOPUS: 2-s2.0-85073899138, DOI: [10.1109/MECO.2019.8760044](https://doi.org/10.1109/MECO.2019.8760044).
- C73. Giorgi, N. R. Bettin, S. Ermini, F. Montefoschi, A. Rizzo, “An Iris+Voice Recognition System for a Smart Doorbell”, *IEEE 8th Mediterranean Conf. on Embedded Computing (MECO)*, June 2019, pp. 419-422, ISBN: 978-1-7281-1740-9, ISSN: 2377-5475, SCOPUS: 2-s2.0-85073892739, DOI: [10.1109/MECO.2019.8760187](https://doi.org/10.1109/MECO.2019.8760187).
- C72. Giorgi, D. R. Oro, S. Ermini, F. Montefoschi, A. Rizzo, “Embedded Face Analysis for Smart Videosurveillance”, *IEEE 8th Mediterranean Conf. on Embedded Computing (MECO)*, June 2019, pp. 403-407, ISBN: 978-1-7281-1740-9, ISSN: 2377-5475, SCOPUS: 2-s2.0-85073885705, DOI: [10.1109/MECO.2019.8760200](https://doi.org/10.1109/MECO.2019.8760200).
- C71. R. Giorgi, G. Mariotti, “**WebRISC-V: a Web-Based Education-Oriented RISC-V Pipeline Simulation Environment**”, *ACM Workshop on Computer Architecture Education (WCAE-19)*, Phoenix, AZ, (USA), June 2019, pp. 1-6, ISBN: 978-1-4503-6842-1/19/06, SCOPUS: 2-s2.0-8507127341, DOI: [10.1145/3338698.3338894](https://doi.org/10.1145/3338698.3338894).
- C70. R. Giorgi, F. Khalili, M. Procaccini, “A Design Space Exploration Tool Set for Future 1K-core High-Performance Computers”, *ACM Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO)*, Valencia, Spain, Jan. 2019, pp. 1-6, ISBN: 978-1-4503-6260-3, SCOPUS: 2-s2.0-85066922404, DOI: [10.1145/3300189.3300195](https://doi.org/10.1145/3300189.3300195).
- C69. R. Giorgi, F. Khalili, M. Procaccini, “Analyzing the Impact of Operating System Activity of different Linux Distributions in a Distributed Environment”, *IEEE Euromicro Int.l Conf. on Parallel, Distributed, and Network-Based Processing*, Pavia, Italy, Feb. 2019, pp. 422-429, ISBN: 978-1-7281-1644-0, SCOPUS: 2-s2.0-85063904172, DOI: [10.1109/EMPDP.2019.8671562](https://doi.org/10.1109/EMPDP.2019.8671562).
- C68. R. Giorgi, M. Procaccini, “Bridging a Data-Flow Execution Model to a Simple Programming Model”, *IEEE Proc. of the Int.l Conf. on High Performance Computing and Simulation (HPCS)*, Dublin, Ireland, July 2019, pp. 165-168, ISBN: 978-1-7281-4484-9, SCOPUS: 2-s2.0-85092043656, DOI: [10.1109/HPCS48598.2019.9188183](https://doi.org/10.1109/HPCS48598.2019.9188183).
- C67. R. Giorgi, F. Khalili, M. Procaccini, “**AXIOM: A Scalable, Efficient and Reconfigurable Embedded Platform**”, *IEEE Proc. Design, Automation and Test in Europe (DATE)*, Florence, Italy, Mar. 2019, pp. 1-6, ISBN: 978-3-9819263-3-0, SCOPUS: 2-s2.0-85063874249, DOI: [10.23919/DATE.2019.8715168](https://doi.org/10.23919/DATE.2019.8715168).
- C66. R. Giorgi, F. Khalili, M. Procaccini, “Energy Efficiency Exploration on the ZYNQ Ultrascale+”, *IEEE Proc. 30th Int.l Conf. on Microelectronics (ICM)*, Sousse, Tunisia, Dec. 2018, pp. 52-55, ISBN: 978-1-5386-8166-4, SCOPUS: 2-s2.0-85065744778.
- C65. R. Giorgi, “AXIOM: A 64-bit reconfigurable hardware/software platform for scalable embedded computing”, *IEEE 6th Mediterranean Conf. on Embedded Computing (MECO)*, June 2017, pp. 113-116, ISBN: 978-1-5090-6741-1, SCOPUS: 2-s2.0-85027066268, DOI: [10.1109/MECO.2017.7977173](https://doi.org/10.1109/MECO.2017.7977173).
- C64. A. Rizzo, F. Montefoschi, M. Caporali, A. Gisoni, G. Burrelli, R. Giorgi, “Rapid Prototyping IoT Solutions Based on Machine Learning”, *Proc. European Conf. on Cognitive Ergonomics 2017*, New York, NY, USA, 2017, pp. 4, ISBN: 978-1-4503-5256-7, SCOPUS: 2-s2.0-85033447501, DOI: [10.1145/3121283.3121291](https://doi.org/10.1145/3121283.3121291).
- C63. S. Mazumdar, E. Ayguade, N. Bettin, S. Bueno J. and Ermini, A. Filgueras, D. Jimenez-Gonzalez, C. Martinez, X. Martorell, F. Montefoschi, D. Oro, D. Pnevmatikatos, A. Rizzo, D. Theodoropoulos, R. Giorgi, “AXIOM: A Hardware-Software Platform for Cyber Physical Systems”, *2016 Euromicro Conf. on Digital System Design (DSD)*, Aug 2016, pp. 539-546, ISBN: 978-1-5090-2816-0, ISSN: N/A, SCOPUS: 2-s2.0-84998953548, WOS:000386638800070, INSPEC: 16413648, DOI: [10.1109/DSD.2016.80](https://doi.org/10.1109/DSD.2016.80).

- C62. R. Giorgi, “Exploring Dataflow-based Thread Level Parallelism in Cyber-physical Systems”, *Proc. ACM Int.l Conf. on Computing Frontiers*, New York, NY, USA, 2016, pp. 6, ISBN: 978-1-4503-4128-8, SCOPUS: 2-s2.0-84978496726, DOI: [10.1145/2903150.2906829](https://doi.org/10.1145/2903150.2906829).
- C61. C. Alvarez, E. Ayguade, J. Bueno, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, N. Navarro, D. Theodoropoulos, D. Pnevmatikatos, C. Scordino, P. Gai, C. Segura, C. Fernandez, D. Oro, J. Saeta, P. Passera, A. Pomella, A. Rizzo, R. Giorgi, “The AXIOM Software Layers”, *IEEE Proc. 18th EUROMICRO-DSD*, Aug. 2015, pp. 117-124, ISBN: 978-1-4673-8035-5, SCOPUS: 2-s2.0-84958165723, WOS:000382382300016, DOI: [10.1109/DSD.2015.52](https://doi.org/10.1109/DSD.2015.52).
- C60. G. Buresi, R. Giorgi, “A Field Experience for a Vehicle Recognition System using Magnetic Sensors”, *IEEE MECO 2015*, Budva, Montenegro, June 2015, pp. 178-181, **Best student-paper award**, ISBN: 978-1-4799-8999-7, SCOPUS: 2-s2.0-84961382637, WOS:000380406100041, INSPEC: 7181897, DOI: [10.1109/MECO.2015.7181897](https://doi.org/10.1109/MECO.2015.7181897).
- C59. L. Verdoscia, R. Vaccaro, R. Giorgi, “A matrix multiplier case study for an evaluation of a configurable Dataflow-Machine”, *ACM CF'15 - LP-EMS*, May 2015, pp. 1-6, ISBN: 978-1-4503-3358-0, SCOPUS: 2-s2.0-84969776968, DOI: [10.1145/2742854.2747287](https://doi.org/10.1145/2742854.2747287).
- C58. N. Ho, A. Mondelli, A. Scionti, M. Solinas, A. Portero, R. Giorgi, “Enhancing an x86_64 Multi-Core Architecture with Data-Flow Execution Support”, *ACM Computing Frontiers*, Ischia, Italy, May 2015, pp. 1-2, ISBN: 978-1-4503-3358-0, SCOPUS: 2-s2.0-84969802071, DOI: [10.1145/2742854.2742896](https://doi.org/10.1145/2742854.2742896).
- C57. R. Giorgi, “Scalable Embedded Systems: Towards the Convergence of High-Performance and Embedded Computing”, *Proc. 13th IEEE/IFIP Int.l Conf. on Embedded and*, Oct. 2015, pp. 148-153, SCOPUS: 2-s2.0-84963800598, WOS:000380405500019, INSPEC: 7363629, DOI: [10.1109/EUC.2015.34](https://doi.org/10.1109/EUC.2015.34).
- C56. R. Giorgi, “Accelerating Haskell on a Dataflow Architecture: a case study including Transactional Memory”, *Proc. Int.l Conf. on Computer Eng. and Applications*, Dubai, UAE, Feb. 2015, pp. 91-100, ISBN: 978-1-61804-276-7, ISSN: 1790-5109.
- C55. D. Theodoropoulos, D. Pnevmatikatos, C. Alvarez, E. Ayguade, J. Bueno, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, N. Navarro, C. Segura, C. Fernandez, D. Oro, J. Saeta, P. Gai, C. Scordino, A. Rizzo, R. Giorgi, “The AXIOM project (Agile, eXtensible, fast I/O Module)”, *IEEE Proc. 15th Int.l Conf. on Embedded Computer Systems: Architecture, MOdeling and Simulation*, July 2015, pp. 262-269, SCOPUS: 2-s2.0-84963649776, WOS:000380507900035, DOI: [10.1109/SAMOS.2015.7363684](https://doi.org/10.1109/SAMOS.2015.7363684).
- C54. A. Mondelli, N. Ho, A. Scionti, M. Solinas, A. Portero, R. Giorgi, “Dataflow Support in x86-64 Multicore Architectures through Small Hardware Extensions”, *IEEE Proc. DSD*, August 2015, pp. 526-529, SCOPUS: 2-s2.0-84958159285, WOS:000382382300075, DOI: [10.1109/DSD.2015.62](https://doi.org/10.1109/DSD.2015.62).
- C53. A. Scionti, S. Kavvadias, R. Giorgi, “Dynamic Power Reduction in Self-Adaptive Embedded Systems through Benchmark Analysis”, *IEEE MECO 2014*, Budva, Montenegro, June 2014, pp. 62-65, ISBN: 978-9940-9436-3-9, SCOPUS: 2-s2.0-84912061826, DOI: [10.1109/MECO.2014.6862659](https://doi.org/10.1109/MECO.2014.6862659).
- C52. I. Branovic, R. Popovic, N. Jovanovic, R. Giorgi, B. Nikolic, M. Zivkovic, “Integration of simulators in virtual 3D computer science classroom”, *Global Engineering Education Conf. (EDUCON), 2014 IEEE*, April 2014, pp. 1164-1167, SCOPUS: 2-s2.0-85002213784, DOI: [10.1109/EDUCON.2014.7096837](https://doi.org/10.1109/EDUCON.2014.7096837).
- C51. L. Verdoscia, R. Vaccaro, R. Giorgi, “A Clockless Computing System based on the Static Dataflow Paradigm”, *Proc. IEEE Int.l Workshop on Data-Flow Execution Models for Extreme Scale Computing (DFM-2014)*, Edmonton, Canada, Aug. 2014, pp. 30-37, ISBN: 978-147998095-6, SCOPUS: 2-s2.0-84949924153, WOS:000380554400005, DOI: [10.1109/DFM.2014.10](https://doi.org/10.1109/DFM.2014.10).
- C50. N. Ho, A. Portero, M. Solinas, A. Scionti, A. Mondelli, P. Faraboschi, R. Giorgi, “Simulating a Multi-core x86-64 Architecture with Hardware ISA Extension Supporting a Data-Flow Execution Model”, *IEEE Proc. AIMS-2014*, Madrid, Spain, Nov. 2014, pp. 264-269, ISBN: 978-1-4799-7600-3, SCOPUS: 2-s2.0-84939287422, WOS:000380431100046, DOI: [10.1109/AIMS.2014.41](https://doi.org/10.1109/AIMS.2014.41).
- C49. R. Giorgi, P. Faraboschi, “An Introduction to DF-Threads and their Execution Model”, *IEEE MPP*, Paris, France, Oct. 2014, pp. 60-65, ISBN: 978-1-4799-7014-8, SCOPUS: 2-s2.0-84939287413, INSPEC: 14792609, DOI: [10.1109/SBAC-PADW.2014.30](https://doi.org/10.1109/SBAC-PADW.2014.30).
- C48. M. Solinas, M. Badia, F. Bodin, A. Cohen, P. Evripidou, P. Faraboschi, B. Fechner, G. Gao, A. Garbade, S. Girbal, D. Goodman, B. Khan, S. Koliaï, F. Li, M. Luján, A. Mendelson, L. Morin, N. Navarro, A. Pop, P. Trancoso, T. Ungerer, M. Valero, S. Weis, S. Zuckerman, R. Giorgi, “The TERAFLUX project: Exploiting the dataflow paradigm in next generation teradevices”, *IEEE Proc. 16th EUROMICRO-DSD*, Santander, Spain, no. 6628287, 2013, pp. 272-279, ISBN: 978-0-7695-5074-9, ISSN: N/A, SCOPUS: 2-s2.0-84890041280, WOS:000337235200036, DOI: [10.1109/DSD.2013.39](https://doi.org/10.1109/DSD.2013.39).

- C47. G. Keramidas, S. Wong, F. Anjam, A. Brandon, R. Seedorf, C. Scordino, L. Carro, D. Matos, R. Giorgi, S. Kavvadias, S. McKee, B. Goel, V. Spiliopoulos, “[Embedded Reconfigurable Computing: the ERA Approach](#)”, *Proc. 11th IEEE Int.l Conf. on Industrial Informatics*, Bochum, Germany, July 2013, pp. 827-832, SCOPUS: 2-s2.0-84927611964, INSPEC: 14563415, DOI: [10.1109/INDIN.2013.6889116](#).
- C46. S. Wong, L. Carro, S. Kavvadias, G. Keramidas, F. Papariello, C. Scordino, R. Giorgi, S. Kaxiras, “[Embedded reconfigurable architectures](#)”, *ACM Proc. 2012 international conference on Compilers, architectures and synthesis for embedded systems (CASES)*, New York, NY, USA, 2012, pp. 2, ISBN: 978-1-4503-1424-4, ISSN: N/A, SCOPUS: 2-s2.0-84869001529, WOS:000324163200029, DOI: [10.1145/2380403.2380444](#).
- C45. A. Portero, A. Scionti, Z. Yu, P. Faraboschi, C. Concatto, L. Carro, A. Garbade, S. Weis, T. Ungerer, R. Giorgi, “[Simulating the Future kilo-x86-64 core Processors and their Infrastructure](#)”, *45th Annual Simulation Symp. (ANSS12)*, Orlando, FL, Mar 2012, pp. 62-67, ISBN: 978-1-61839-784-3, SCOPUS: 2-s2.0-84876493480.
- C44. R. Giorgi, “[TERAFLUX: Exploiting Dataflow Parallelism in Teradevices](#)”, *ACM Computing Frontiers*, Cagliari, Italy, May 2012, pp. 303-304, ISBN: 978-1-4503-1215-8, SCOPUS: 2-s2.0-84862644101, DOI: [10.1145/2212908.2212959](#).
- C43. R. Giorgi, A. Scionti, A. Portero, P. Faraboschi, “[Architectural Simulation in the Kilo-core Era](#)”, *Architectural Support for Programming Languages and Operating Systems (ASPLOS 2012)*, poster presentation, London, UK, Mar 2012, pp. 1-3.
- C42. Z. Yu, A. Righi, R. Giorgi, “[A Case Study on the Design Trade-off of a Thread Level Data Flow based Many-core Architecture](#)”, *Future Computing*, Rome, Italy, Sept. 2011, pp. 100-106, **Best paper award**, ISBN: 978-1-61208-154-0.
- C41. S. Wong, A. Brandon, F. Anjam, R. Seedorf, R. Giorgi, Z. Yu, N. Puzovic, S. McKee, Magnus Sjaelander and Georgios Keramidas, “[Early Results from ERA – Embedded Reconfigurable Architectures](#)”, *9th IEEE Int.l Conf. on Industrial Informatics (INDIN)*, Lisbon, Portugal, Jul 2011, pp. 816-822, ISBN: 978-1-4577-0433-8, ISSN: 1935-4576, SCOPUS: 2-s2.0-80055020953, WOS:000298743300125, DOI: [10.1109/INDIN.2011.6034998](#).
- C40. S. Weis, A. Garbade, J. Wolf, B. Fechner, A. Mendelson, R. Giorgi, T. Ungerer, “[A Fault Detection and Recovery Architecture for a Teradevice Dataflow System](#)”, *Proc. IEEE Int.l Workshop on Data-Flow Execution Models for Extreme Scale Computing (DFM)*, Oct. 2011, pp. 38-44, ISBN: 978-1-4673-0709-3, SCOPUS: 2-s2.0-84860536526, INSPEC: 12654360, DOI: [10.1109/DFM.2011.9](#).
- C39. R. Giorgi, “[TERAFLUX: Ideas for the Future Many-Cores](#)”, *ODES: Workshop on Optimizations for DSP and Embedded Systems*, Apr. 2011, pp. 38-38.
- C38. N. Puzovic, S. McKee, R. Eres, A. Zaks, P. Gai, S. Wong, R. Giorgi, “[A Multi-Pronged Approach to Benchmark Characterization](#)”, *IEEE Int.l Conf. on Cluster Computing (CLUSTER2010)*, Heraklion, Greece, Sept. 2010, pp. 1-4, ISBN: 978-1-4244-8396-9, SCOPUS: 2-s2.0-78649899217, DOI: [10.1109/CLUSTERWKSP.2010.5613090](#).
- C37. C. M. B. Alioto, P. Bennati, R. Giorgi, “[Exploiting Locality to Improve Leakage Reduction in Embedded Drowsy I-Caches at Same Area/Speed](#)”, *IEEE Int.l Symp. on Circuits and Systems (ISCAS)*, Paris, France, May 2010, pp. 37-40, ISBN: 978-1-4244-5309-2, ISSN: 0271-4302, SCOPUS: 2-s2.0-77955986564, WOS:000287216000010, DOI: [10.1109/ISCAS.2010.5537105](#).
- C36. K. Stavrou, D. Pavlou, M. Nikolaides, P. Petrides, P. Evripidou, P. Trancoso, Z. Popovic, R. Giorgi, “[Programming Abstractions and Toolchain for Dataflow Multithreading Architectures](#)”, *IEEE Proc. Eighth Int.l Symp. on Parallel and Distributed Computing (ISPDC 2009)*, Lisbon, Portugal, July 2009, pp. 107-114, ISBN: 978-0-7695-3680-4, ISSN: N/A, SCOPUS: 2-s2.0-74349119578, WOS:000275741200013, DOI: [10.1109/ISPDC.2009.35](#).
- C35. R. Giorgi, Z. Popovic, N. Puzovic, “[Implementing Fine/Medium Grained TLP Support in a Many-Core Architecture](#)”, *Proc. 9th Int.l Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation, SAMOS 2009*, Samos, Greece, July 2009, pp. 78-87, ISBN: 978-3-642-03137-3, ISSN: 0302-9743, SCOPUS: 2-s2.0-70350359181, WOS:000270018700009, DOI: [10.1007/978-3-642-03138-0.9](#).
- C34. R. Giorgi, Z. Popovic, N. Puzovic, “[Exploiting DMA to enable non-blocking execution in Decoupled Threaded Architecture](#)”, *Proc. IEEE Int.l Symp. on Parallel and Distributed*, Rome, Italy, May 2009, pp. 2197-2204, ISBN: 978-1-4244-3751-1, ISSN: 1530-2075, SCOPUS: 2-s2.0-70449913551, WOS:000272993601035, DOI: [10.1109/IPDPS.2009.5161111](#).
- C33. R. Giorgi, Z. Popovic, N. Puzovic, “[Introducing hardware TLP support for the Cell processor](#)”, *Proc. IEEE Int.l Workshop on Multi-Core Computing Systems*, Fukuoka, Japan, Mar. 2009, pp. 657-662, ISBN: 978-1-4244-3569-2, ISSN: N/A, SCOPUS: 2-s2.0-70349735998, WOS:000272961700096, DOI: [10.1109/CISIS.2009.177](#).
- C32. R. Giorgi, P. Bennati, “[Reducing Leakage through Filter Cache](#)”, *IEEE Proc. 11th EUROMICRO-DSD*, Parma, Italy, Sept. 2008, pp. 334-341, ISBN: 978-1-59593-753-7, ISSN: N/A, SCOPUS: 2-s2.0-57649239603, WOS:000264279400043, DOI: [10.1109/DSD.2008.123](#).

- C31. R. Giorgi, Z. Popovic, N. Puzovic, A. Azavedo, B. Juurlink, “Analyzing Scalability of Deblocking Filter of H.264 via TLP exploitation in a new many-core architecture”, *IEEE Proc. 11th EUROMICRO-DSD*, Parma, Italy, Sept. 2008, pp. 189-194, ISBN: 978-1-59593-753-7, ISSN: N/A, SCOPUS: 2-s2.0-57649199756, WOS:000264279400025, DOI: [10.1109/DSD.2008.93](https://doi.org/10.1109/DSD.2008.93).
- C30. R. Giorgi, P. Bennati, “Filtering drowsy instruction cache to achieve better efficiency”, *SAC '08: Proc. 2008 ACM symposium on Applied computing*, New York, NY, USA, Mar. 2008, pp. 1554-1555, ISBN: 978-1-59593-753-7, ISSN: N/A, SCOPUS: 2-s2.0-56749156882, WOS:000268392201137, DOI: [10.1145/1363686.1364050](https://doi.org/10.1145/1363686.1364050).
- C29. R. Giorgi, P. Bennati, “Reducing leakage in power-saving capable caches for embedded systems by using a filter cache”, *Proc. ACM MEDEA*, Brasov, Romania, Sept. 2007, pp. 105-112, ISBN: 978-1-59593-807-7, SCOPUS: 2-s2.0-77954436701, DOI: [10.1145/1327171.1327183](https://doi.org/10.1145/1327171.1327183).
- C28. R. Giorgi, Z. Popovic, N. Puzovic, “DTA-C: A Decoupled multi-Threaded Architecture for CMP Systems”, *Proc. IEEE SBAC-PAD*, Gramado, Brasil, Oct. 2007, pp. 263-270, ISBN: 0-7695-23014-1, ISSN: 1550-6533, SCOPUS: 2-s2.0-47249097035, WOS:000252137000031, INSPEC: 9855214, DOI: [10.1109/SBAC-PAD.2007.27](https://doi.org/10.1109/SBAC-PAD.2007.27).
- C27. P. Bennati, R. Giorgi, “JCacheSim: simulatore visuale di gerarchia di memoria con interprete per programmi MIPS”, *AICA Didamatica*, Cagliari, Italy, May 2006, pp. 105-114.
- C26. S. Bartolini, P. Bennati, R. Giorgi, “BLUESIGN: traduttore multimediale portatile per non udenti”, *AICA Didamatica*, Cagliari, Italy, May 2006, pp. 17-24.
- C25. S. Bartolini, P. Bennati, R. Giorgi, “Bluesign-2, il nuovo visualizzatore portatile per la Lingua Italiana dei Segni”, *Atti del 51esimo Convegno Nazionale di Studio ed Aggiornamento AIES*, S. Pellegrino (BG), Italy, Aug. 2005, pp. 140-145.
- C24. I. Branovic, R. Giorgi, E. Martinelli, “WebMIPS: A New Web-Based MIPS Simulation Environment for Computer Architecture Education.”, *IEEE Workshop on Computer Architecture Education (WCAE-04)*, Munich, Germany, June 2004, pp. 93-98, SCOPUS: 2-s2.0-84897704899, DOI: [10.1145/1275571.1275596](https://doi.org/10.1145/1275571.1275596).
- C23. S. Bartolini, P. Bennati, R. Giorgi, “Sistema per la traduzione in Lingua Italiana dei Segni: Blue Sign Translator / Wireless Sign System”, *Atti del 50esimo Convegno Nazionale di Studio ed Aggiornamento AIES*, Chianciano Terme - Siena, Italy, Aug. 2004, pp. 203-212.
- C22. S. Bartolini, I. Branovic, R. Giorgi, E. Martinelli, “A Performance Evaluation of ARM ISA Extension for Elliptic Curve Cryptography over Binary Finite Fields”, *IEEE 16th Symp. on Computer Architecture and High Performance Computing (SBAC-PAD-04)*, Foz do Iguacu, Brasil, Oct. 2004, pp. 238-245, ISBN: 0-7695-2240-8, ISSN: 1550-6533, SCOPUS: 2-s2.0-16244420738, WOS:000225222600030, DOI: [10.1109/SBAC-PAD.2004.5](https://doi.org/10.1109/SBAC-PAD.2004.5).
- C21. P. Foglia, R. Giorgi, C. Prete, “Speeding-up Multiprocessors Running DSS Workloads through Coherence Protocols”, *2nd Workshop on Hardware Software Support for Parallel and*, New Orleans, LA, USA, Sept. 2003, pp. 124-149.
- C20. I. Branovic, R. Giorgi, E. Martinelli, “Memory Performance of Public-Key cryptography Methods in Mobile Environments”, *ACM SIGARCH Workshop on MEMory performance: DEALing with Applications, systems and architecture (MEDEA-03)*, New Orleans, LA, USA, Sept. 2003, pp. 24-31.
- C19. P. Foglia, R. Giorgi, C. Prete, “Boosting the Performance of Three-Tier Web Servers Deploying SMP Architecture”, *Springer-Verlag LNCS Workshop on Web Engineering (WWE-02)*, Pisa, Italy, vol. 2376, May 2002, pp. 134-146, ISBN: 3-540-44177-8, ISSN: 0302-9743, SCOPUS: 2-s2.0-84885225152, WOS:000187251900012, DOI: [N/A](https://doi.org/N/A).
- C18. I. Branovic, R. Giorgi, C. A., “Web-based training on Computer Architecture: The case for JCacheSim”, *IEEE Workshop on Computer Architecture Education (WCAE-02)*, Anchorage, AK, USA, May 2002, pp. 56-60, SCOPUS: 2-s2.0-84969262570.
- C17. K. Kavi, J. Arul, R. Giorgi, “Performance Evaluation of a Non-Blocking Multithreaded Architecture for Embedded, Real-Time and DSP Applications”, *14th Intl Conf. on Parallel and Distributed Computing Systems (ISCA-PDCS-01)*, Richardson, TX, USA, Aug. 2001, pp. 365-371, ISBN: 1-880843-39-0, ISSN: N/A, WOS:000179289500059, DOI: [N/A](https://doi.org/N/A).
- C16. P. Foglia, R. Giorgi, C. Prete, “OS Effects on Memory Hierarchy of a SMP Multiprocessor Running a DBMS Workload”, *Intl Conf. on Advances in Infrastructure for E-Business, Science, and Education (SSGRR-01)*, L'Aquila, Italy, Aug. 2001, pp. 1-8 (cdrom), ISBN: 88-85280-61-7.
- C15. P. Foglia, R. Giorgi, C. Prete, “Accelerating DSS Workloads through Coherence Protocols”, *ACM Workshop on Caching and Coherence Consistency (WC3-01)*, Sorrento, Italy, June 2001, pp. G.1-G.8.
- C14. P. Foglia, R. Giorgi, C. Prete, “Performance Analysis of Parallel Applications Running on SMP”, *Intl Conf. on Parallel and Distributed Processing Techniques and Applications (PDPTA-01)*, Las Vegas, NV, USA, vol. IV, June 2001, pp. 1634-1640, ISBN: 1-892512-70-X, ISSN: N/A, WOS:000174014500247, DOI: [N/A](https://doi.org/N/A).

- C13. P. Foglia, R. Giorgi, C. Prete, “Evaluating Optimizing for Multiprocessors E-Commerce Server Running TPC-W Workload”, *IEEE Proc. 34th Annual Hawaii Intl Conf. on System Sciences (HICSS-34)*, Maui, Hawaii, USA, vol. 7, Jan. 2001, pp. 2544-2552, ISBN: 0-7695-0981-9, SCOPUS: 2-s2.0-0034974343, INSPEC: 6859484, DOI: [10.1109/HICSS.2001.927077](https://doi.org/10.1109/HICSS.2001.927077).
- C12. K. Kavi, R. Giorgi, J. Arul, “Comparing Execution Performance of Scheduled Dataflow Architecture with RISC Processors”, *Proc. 13th ISCA Parallel and Distributed Computing Systems Conf. (ISCA-PDCS-00)*, Las Vegas, NV, USA, Aug. 2000, pp. 41-47, ISBN: 1-880843-34-X, ISSN: N/A, WOS:000179773600007, DOI: [N/A](https://doi.org/N/A).
- C11. P. Foglia, R. Giorgi, C. Prete, “Performance Analysis of Electronic Commerce Multiprocessor Servers”, *IEEE Proc. 33th Annual Hawaii Intl Conf. on System Sciences (HICSS-33)*, Maui, Hawaii, USA, Jan. 2000, pp. 2214-2222, ISBN: 0-7695-0493-0, SCOPUS: 2-s2.0-0033885039.
- C10. R. Giorgi, C. Prete, “A Coherence Protocol for the Elimination of Passive Sharing in Single and Multiple Threaded Shared-Bus Shared-Memory Multiprocessors”, *Eighth Workshop on Scalable Shared Memory Multiprocessors (WSSMM-99)*, Atlanta, Georgia, May 1999, pp. 29.
- C9. P. Foglia, R. Giorgi, C. Prete, “Process Migration Effects on Memory Performance of Multiprocessor Web-Server”, *Springer-Verlag LNCS Proc. High Performance Computing Conf. (HIPC-99)*, Calcutta, India, vol. 1745, Dec. 1999, pp. 133-142, ISBN: 3-540-66907-8, SCOPUS: 2-s2.0-70349176898.
- C8. R. Giorgi, C. Prete, “An Educational Environment for Designing and Performance Tuning of Embedded Systems”, *IEEE Workshop on Computer Architecture Education (WCAE-98)*, Barcelona, Spain, June 1998, pp. VII/A.1-6, ISBN: 978-1-4503-4736-5, SCOPUS: 2-s2.0-84977079593, DOI: [10.1145/1275182.1275211](https://doi.org/10.1145/1275182.1275211).
- C7. P. Foglia, R. Giorgi, C. Prete, “Analysis of Sharing Overhead in Shared Memory Multiprocessors”, *IEEE Proc. 31st Annual Hawaii Intl Conf. on System Sciences (HICSS-31)*, Big Island, Hawaii, USA, vol. 7, Jan. 1998, pp. 776-777, ISBN: 0-8186-8255-8, ISSN: 1060-3425, SCOPUS: 2-s2.0-0031612524, WOS:000072158800092, DOI: [N/A](https://doi.org/N/A).
- C6. R. Giorgi, C. Prete, G. Prina, “An Educational Environment for Program Behavior Analysis and Cache Memory Design”, *IEEE Proceedings Intl Conf. on Frontiers in Education (FIE-97)*, Pittsburgh, PA, USA, Nov. 1997, pp. 1243-1248, ISBN: 0-7803-4087-6, ISSN: 0190-5848, SCOPUS: 2-s2.0-0031335181, WOS:A1997BJ93M00289, DOI: [N/A](https://doi.org/N/A).
- C5. R. Giorgi, C. Prete, G. Prina, “An approach for investigating design and tuning performance of embedded systems”, *EAEIE Proc. Intl Conf. on Innovation and Quality in Education for Electrical and Information Engineering*, Edinburgh, Scotland, UK, June 1997, pp. G1.15-20.
- C4. R. Giorgi, P. Foglia, C. Prete, “Bus Utilization Analysis of Multithreaded Shared-Bus Multiprocessors: Initial Results”, *IASTED Proc. 9th Intl Conf. on Parallel and Distributed Computing and Systems (IPDCS-97)*, Washington, DC, USA, Oct. 1997, pp. 24-29, ISBN: 0-88986-240-0.
- C3. R. Giorgi, C. Prete, G. Prina, “Cache Memory Design for Embedded Systems Based on Program Locality Analysis”, *IEEE Proc. Intl Conf. on Microelectronic System Education (MSE-97)*, Arlington, VA, USA, July 1997, pp. 16-18, ISBN: 0-8186-7996-4, ISSN: N/A, SCOPUS: 2-s2.0-0030681889, WOS:A1997BJ30F00007, DOI: [10.1109/MSE.1997.612528](https://doi.org/10.1109/MSE.1997.612528).
- C2. R. Giorgi, C. Prete, G. Prina, L. Ricciardi, “A Workload Generation Environment for Trace-Driven Simulation of Shared-Bus Multiprocessor”, *IEEE Proc. 30th Hawaii Intl Conf. on System Sciences (HICSS-30)*, Maui, Hawaii, vol. 1, Jan. 1997, pp. 266-275, Best mini-track paper award, ISBN: 0-8186-7734-1, ISSN: 1060-3425, SCOPUS: 2-s2.0-0031348221, WOS:000073324200030, DOI: [10.1109/HICSS.1997.667272](https://doi.org/10.1109/HICSS.1997.667272).
- C1. R. Giorgi, C. Prete, G. Prina, L. Ricciardi, “A Hybrid Approach to Trace Generation for Performance Evaluation of Shared-Bus Multiprocessors”, *IEEE Proc. 22nd EuroMicro Intl Conf. (EM-96)*, Prague, Czech Republic, Sept. 1996, pp. 207-214, ISBN: 0-8186-7487-3, DOI: [10.1109/EURMIC.1996.546384](https://doi.org/10.1109/EURMIC.1996.546384).

11 Papers: Miscellaneous

- M5. V. Antunovic, I. Bozovic, S. Cloetingh, N. Dakovic, N. Delilovic, F. Djukanovic and M., G. B., A. R. and Kavcic, E. Kondorosi, M. Lazic, H. Maurer, O. Mencer, F. Mesinger, M. Mihaljevic, V. Milutinovic, D. Mircevski, L. Moutinho, Z. Ognjanovic, P. Papale, O. Petersen, M. Radovic-Markovic, S. Rizvic, J. Salom, A. Verkhatsky, G. Vunjak-Novakovic, B. Zlokovic, “Proverbial Opinions of Selected Experts: From Past Experiences to Future Directions”, *IPSI Trans. Advanced Research*, vol. 16, Dec 2019, pp. 50-61.
- M4. R. Giorgi, Z. Popovic, N. Puzovic, “Memory access decoupling in a multithreaded architecture”, *WIRTES 2007 - Primo Workshop Italiano su Real-Time Embedded Systems*, Pisa, Italy, July 2007, pp. 1-11.

- M3. S. Bartolini, R. Giorgi, E. Martinelli, Z. Popovic, “Tiled Architectures and Recent Proposals for Chip”, , no. 5, May 2005, pp. 23.
- M2. R. Giorgi, “Evaluation of a Coherence Protocol for Eliminating Passive Sharing in Shared-Bus Multithreaded Multiprocessors”, *University of Pisa, Dept. Ingegneria della Informazione*, Ph.D. Thesis, Pisa, Italy, Jan. 1999, pp. 84.
- M1. R. Giorgi, “Valutazione delle Prestazioni di Sistemi Multiprocessore Basata sull’Analisi di Tracce Reali”, *University of Pisa, Dept. Ingegneria della Informazione*, MS Thesis, Pisa, Italy, July 1995, pp. 96.

12 Posters

- P24. A. Sahebi, R. Giorgi, “GLUON, The High-Speed Inexpensive and Easy Interconnect Solution”, *HiPEAC ACACES 2020 Online Event*, Fiuggi, Italy, July 2020, (online poster).
- P23. M. Procaccini, R. Giorgi, “An Extended Tracing System for the COTSon Simulator”, *HiPEAC ACACES-2020*, Fiuggi, Italy, July 2020, (poster).
- P22. G. Mariotti, R. Giorgi, “WebRISC-V: A RISC-V Educational Simulator featuring RV64IM, Pipeline and Web-Based UI”, *HiPEAC ACACES-2020*, Fiuggi, Italy, July 2020, pp. 19-22, (Online poster), ISBN: 978-90-784270-0-1.
- P21. R. Khalili and Giorgi, “A Dynamic Load Balancer for a Cluster of FPGA SoCs”, *HiPEAC ACACES-2020*, Fiuggi, Italy, July 2020, (Online poster).
- P20. A. Sahebi, L. Verdoscia, R. Giorgi, “A Data-Flow Approach To Accelerate Real-Valued Fast Fourier Transform”, *HiPEAC ACACES-2019*, Fiuggi, Italy, July 2019, pp. 155-158, (poster), ISBN: 978-88-905806-7-3.
- P19. M. Procaccini, R. Giorgi, “x86_64 vs Aarch64 Performance Validation with COTSon”, *HiPEAC ACACES-2019*, Fiuggi, Italy, July 2019, pp. 261-264, (poster), ISBN: 978-88-905806-7-3.
- P18. F. Khalili, R. Giorgi, “A Soft-IP for Performance Measuring of the Zynq Ultrascale+ CPU/FPGA interface”, *HiPEAC ACACES-2019*, Fiuggi, Italy, July 2019, pp. 5-8, (poster), ISBN: 978-88-905806-7-3.
- P17. M. Procaccini, F. Khalili, R. Giorgi, “An FPGA-based Scalable Hardware Scheduler for Data-Flow Models”, *HiPEAC ACACES-2018*, Fiuggi, Italy, July 2018, pp. 1-4, (poster), ISBN: 978-88-905806-6-6.
- P16. F. Khalili, M. Procaccini, R. Giorgi, “Reconfigurable Logic Interface Architecture for CPU-FPGA Accelerators”, *HiPEAC ACACES-2018*, Fiuggi, Italy, July 2018, pp. 1-4, (poster), ISBN: 978-88-905806-6-6.
- P15. R. Giorgi, F. Khalili, M. Procaccini, “An FPGA-based Scalable Hardware Scheduler for Data-Flow Models”, *Intl workshop on FPGAs for Domain Experts (FPODE)*, Limassol, Cyprus, Nov. 2018, pp. 1-1, (poster).
- P14. M. Procaccini, R. Giorgi, “Simulation infrastructure for the next kilo x86-64 Chips”, *HiPEAC ACACES-2017*, Fiuggi, Italy, July 2017, pp. 91-94, (poster), ISBN: 978 88 905806 5 9.
- P13. A. Portero, A. Scionti, M. Solinas, H. Nam, R. Giorgi, “Simulation infrastructure for the next kilo x86-64 Chips”, *HiPEAC ACACES-2012*, Fiuggi, Italy, July 2012, pp. 87-90, (poster), ISBN: 978 90 382 19.
- P12. C. Kang, S. Kavvadias, A. Scionti, C. Scordino, P. Gai, R. Giorgi, “Dynamically Reconfiguring through Phase Detection on FPGA”, *HiPEAC ACACES-2012*, Fiuggi, Italy, July 2012, pp. 149-152, (poster), ISBN: 978 90 382 1987 5.
- P11. Z. Yu, N. Puzovic, A. Portero, R. Giorgi, “Characterizing Phase Behavior for Dynamically Reconfigurable Architectures”, *HiPEAC ACACES-2011*, Fiuggi, Italy, July 2011, pp. 89-92, (poster), ISBN: 978 90 382 17987.
- P10. A. Portero, Z. Yu, R. Giorgi, “T-Star (T*): An x86-64 ISA Extension to support thread execution on many cores”, *HiPEAC ACACES-2011*, Fiuggi, Italy, July 2011, pp. 277-280, (poster), ISBN: 978 90 382 17987.
- P9. R. Giorgi, Z. Popovic, N. Puzovic, “Implementing DTA support in CellSim”, *HiPEAC ACACES-2008*, L’Aquila, Italy, July 2008, pp. 159-162, (poster), ISBN: 978-90-382-1288-3.
- P8. R. Giorgi, Z. Popovic, N. Puzovic, A. Azavedo, B. Juurlink, “Exploiting Parallelism of Deblocking Filter of H.264 on DTA architecture”, *HiPEAC ACACES-2008*, L’Aquila, Italy, July 2008, pp. 55-58, (poster), ISBN: 978-90-382-1288-3.
- P7. R. Giorgi, Z. Popovic, N. Puzovic, “Decoupled Threaded Architecture”, *HiPEAC ACACES-2007*, L’Aquila, Italy, July 2007, pp. 119-121, (poster), ISBN: 97-890-382-1127-5.
- P6. P. Bennati, R. Giorgi, “Adaptive Cache Decay”, *HiPEAC ACACES-2007*, L’Aquila, Italy, July 2007, pp. 1-4, (poster), ISBN: 97-890-382-1127-5.

- P5. R. Giorgi, N. Puzovic, “[Scheduling and NoC Traffic Reduction in T-SDF Architecture](#)”, *HiPEAC ACACES-2006*, L’Aquila, Italy, July 2006, pp. 253-256, (poster), ISBN: 90-382-0981-9.
- P4. R. Giorgi, Z. Popovic, “[Core Design and Scalability of Tiled SDF Architecture](#)”, *HiPEAC ACACES-2006*, L’Aquila, Italy, July 2006, pp. 145-148, (poster), ISBN: 90-382-0981-9.
- P3. S. Bartolini, P. Bennati, R. Giorgi, E. Martinelli, “[Elliptic Curve Cryptography support for ARM based Embedded systems](#)”, *HiPEAC ACACES-2006*, L’Aquila, Italy, July 2006, pp. 13-16, (poster), ISBN: 90-382-0981-9.
- P2. S. Bartolini, R. Giorgi, E. Martinelli, Z. Popovic, “[Recent Proposals for Tiled Architectures Multiprocessors](#)”, *HiPEAC ACACES-2005*, L’Aquila, Italy, July 2005, pp. 47-50, (poster), ISBN: 90-382-0802-2.
- P1. M. Alioto, S. Bartolini, P. Bennati, R. Giorgi, “[New techniques for low power caches](#)”, *HiPEAC ACACES-2005*, L’Aquila, Italy, July 2005, pp. 133-136, (poster), ISBN: 90-382-0802-2.

13 Technical Reports and Deliverables

- D20. R. Giorgi, F. Khalili, F. Montefoschi, M. Procaccini, X. Martorell, D. Jiménez-González, A. C., P. Gai, S. Garzarella, V. Amourianos, D. Theodoropoulos, D. Pnevmatikatos, D. Oro, D. Catani, D. Cardillo, C. Magnani, S. Viola, N. Bettin, A. Pomella, “[Performance and Energy Evaluation of AXIOM](#)”, *AXIOM D7.3*, Siena, Italy, Feb 2018, pp. 1-54, (deliverable).
- D19. P. Gai, S. Garzarella, B. Morelli, M. X., D. Jiménez-González, A. C., F. Procaccini and M. and Khalili, R. Giorgi, “[Final operating system and documentation](#)”, *AXIOM D5.4*, Siena, Italy, Feb 2018, pp. 1-31, (deliverable).
- D18. M. Caporali, A. Rovai, R. Giorgi, “[Final Rep. on AXIOM Events](#)”, *AXIOM D2.4*, Siena, Italy, Feb 2018, pp. 1-28, (deliverable).
- D17. R. Giorgi, S. Viola, “[Design Space Exploration \(DSE\) on the prototype](#)”, *AXIOM D7.2*, Siena, Italy, Feb 2017, pp. 1-36, (deliverable).
- D16. M. Caporali, A. Rovai, R. Giorgi, “[Rep. on AXIOM Events](#)”, *AXIOM D2.2*, Siena, Italy, Feb 2017, pp. 1-59, (deliverable).
- D15. R. Giorgi, “[Design Space Exploration \(DSE\) on the prototype](#)”, *AXIOM D7.1*, Siena, Italy, Jan 2016, pp. 1-38, (deliverable).
- D14. R. Giorgi, “[Initial AXIOM Evaluation Platform \(AEP\) definition and initial tests](#)”, *AXIOM D7.1*, Siena, Italy, Jan 2016, pp. 1-38, (deliverable).
- D13. D. Catani, C. Magnani, X. Martorell, N. Navarro, D. Jiminez-Gonzalez, C. Alvarez, P. Gai, C. Scordino, D. Pnevmatikatos, D. Theodoropoulos, A. Pomella, R. Giorgi, “[Tech. specification of AXIOM boards](#)”, *AXIOM D6.1*, Siena, Italy, Jan 2016, pp. 1-23, (deliverable).
- D12. D. Catani, C. Magnani, X. Martorell, N. Navarro, D. Jiminez-Gonzalez, C. Alvarez, P. Gai, C. Scordino, D. Pnevmatikatos, D. Theodoropoulos, A. Pomella, R. Giorgi, “[Tech. specification of AXIOM boards](#)”, *AXIOM D6.1*, Siena, Italy, Oct 2015, pp. 1-23, (deliverable).
- D11. S. Zuckerman, J. Arteaga, J. Suetterlein, H. Wei, E. Garcia, G. Gao, A. Scionti, R. Giorgi, “[Evaluation of the Codelet Runtime System on a Teradevice](#)”, *TERAFLUX D9.3*, Siena, Italy, May 2014, pp. 1-53, (deliverable).
- D10. A. Scionti, H. Kifle, S. Mazumdar, R. Giorgi, N. Navarro, R. Badia, M. Valero, S. Weis, T. Ungerer, G. Mathou, T. Trancoso, P. Evripidou, A. Fuchs, Y. Weinsberg, P. Faraboschi, B. Khan, Watson, F. I. Li, A. Cohen, S. Zuckerman, J. Arteaga, G. Gao, L. Morin, S. Girbal, “[Final Rep. and Documentation](#)”, *TERAFLUX D7.5*, Siena, Italy, May 2014, pp. 1-100, (deliverable).
- D9. A. Cohen, F. Gindraud, F. Li, A. Pop, R. Badia, N. Navarro, T. Patejko, I. Watson, B. Khan, M. Lujan, R. Giorgi, A. Mondelli, L. Morin, “[Advanced Version of the Compilation Tools](#)”, *TERAFLUX D4.7*, Siena, Italy, May 2014, pp. 1-25, (deliverable).
- D8. R. Badia, D. Jiminez, C. Alvarez, A. Grabade, S. Weis, T. Ungerer, Diavastos, G. A. Mathou, T. Trancoso, P. Evripidou, B. Khan, S. Khan, W. Toms, M. Lujan, I. Watson, R. Giorgi, A. Scionti, B. Jacob, “[Evaluation of the TERAFLUX Abstraction Layer and Fine-tuned Model](#)”, *TERAFLUX D6.4*, Siena, Italy, May 2014, pp. 1-65, (deliverable).
- D7. M. Solinas, A. Scionti, M. Mondelli, N. Ho, A. Portero, S. Kavvadias, M. Bianchini, R. Giorgi, A. Garbade, S. Weis, T. Ungerer, A. Pop, F. Li, A. Cohen, L. Eleftheriades, N. Masrujeh, G. Michael, L. Petrou, A. Diavastos, T. Trancoso, P. Evripidou, N. Navarro, R. Badia, M. Valero, P. Faraboschi, B. Khan, S. Khan, M. Lujan, I. Watson, “[Rep. on knowledge transfer and training](#)”, *TERAFLUX D7.4*, Siena, Italy, Dec. 2012, pp. 1-50, (deliverable).

- D6. R. Giorgi, A. Portero, A. Scionti, A. Garbade, S. Weis, T. Ungerer, “[Power and Thermal Modeling and Fault-injection support](#)”, *TERAFLUX D7.3*, Siena, Italy, Mar. 2012, pp. 1-28, (deliverable).
- D5. C. Christofi, A. Diavastos, G. Michael, G. Mathou, T. Trancoso, P. Evripidou, M. Solinas, A. Scionti, A. Mondelli, H. Nam, A. Portero, R. Giorgi, B. Khan, S. Khan, M. Lujan, I. Watson, F. Yazdanpanah, D. Jimenez, A. Alvarez, Y. Etsion, R. Badia, “[Fine-tuned TERAFLUX Execution Model](#)”, *TERAFLUX D6.3*, Siena, Italy, Dec 2012, pp. 1-34, (deliverable).
- D4. R. Giorgi, A. Portero, C. Concatto, R. Mameesh, Z. Yu, Y. Etsion and L. Villanova and N. Navarro and R. Badia and M. Valero and P. Faraboschi and A. Cohen and D. Shamia and A. Mendelson and A. Garbade and S. Weis and T. Ungerer and P. Trancoso and P. Evripidou and B. Khan and S. Khan and M. Lujan and C. Kirkham and I. Watson, “[Definition of ISA extensions, custom devices and External COTSon API extensions](#)”, *TERAFLUX D7.2*, Siena, Italy, Mar. 2011, pp. 1-78, (deliverable).
- D3. R. Badia, Y. Etsion, R. Gayatri, M. Pavlovic, T. Patejko, D. Goodman, C. Seaton, M. Lujan, I. Watson, A. Portero, R. Giorgi, A. Diavastos, C. Christofi, S. Arandi, G. Michael, T. Trancoso, P. Evripidou, S. Girbal, “[Final report on the characterization and modeling](#)”, *TERAFLUX D2.2*, Siena, Italy, Dec 2011, pp. 1-43, (deliverable).
- D2. S. Arandi, C. Kyriacou, G. Michael, G. Mathou, N. Masrujeh, T. Trancoso, P. Evripidou, R. Giorgi, Z. Yu, S. Collange, S. Scionti, B. Khan, S. Khan, M. Lujan, I. Watson, T. Ungerer, B. Fechner, A. Garbade, S. Weis, “[Advanced TERAFLUX Architecture](#)”, *TERAFLUX D6.2*, Siena, Italy, Dec 2011, pp. 1-49, (deliverable).
- D1. R. Badia, Y. Etsion, J. Labarta, N. Navarro, M. Pavlovic, C. Servat. H. and Villavieja, S. Girbal, M. Ansari, M. Lujan, C. Kirkham, I. Watson, R. Giorgi, A. Portero, A. Cohen, “[Rep. on the reference set of applications chosen, and initial characterization of the applications](#)”, *TERAFLUX D2.1*, Siena, Italy, Dec 2010, pp. 1-44, (deliverable).

14 Intellectual Property

- IP2. S. Bartolini, P. Bennati, R. Giorgi, “BlueSign 2”, *SIAE 24-02-2006/001*, Reg. 24 Feb. 2006.
- IP1. P. Bennati, T. Capasso, V. Di Massa, F. Giallombardo, R. Giorgi, M. Guerrini, E. Maggio, N. Nannetti, “[BlueSign Translator](#)”, *SIAE 002568, Ord. D003454*, Reg. 21 Mar. 2003.

15 Educational and Research Software

- SW8. 2019(June)The WebRISC-V: Web-based RISC-V pipeline simulator <http://www.dii.unisi.it/~giorgi/WebRISC-V>
- Simulates a RISC-V pipeline inside a web browser. The architectural elements are visualized while instructions pass through the pipeline.
 - This is a Bachelor Thesis that I supervised (Gianfranco Mariotti) for the realization of this tool, which led to a publication at the Workshop on Computer Architecture Education.
- SW7. 2015(May) FREESS: The Free SuperScalar simulator <http://www.dii.unisi.it/~giorgi/freess>
- Simulates a simple Superscalar processor step-by-step, visualizing the activity of renaming, instruction window, reorder buffer, load/store queues.
 - I am the author of this educational tool for students. The tool is written from scratch.
- SW6. 2013(Sep) The Dataflow Run Time (DRT) <http://sourceforge.net/projects/drt/>
- A runtime library to code and debug programs that are based on a Thread-Level-Parallelism Instruction Set Extension (TLP ISE).
 - I am the author of this tool which allows to execute programs in a dataflow style by simpling adding a header and using few library calls.
- SW5. 2013(Jun) COTSon Thread Scheduler Unit (TSU) <http://sourceforge.net/p/cotson/code/HEAD/tree/branches/timing-unisi/tsu4/>
- A functional and timing model for an x86_64 based full-system. It uses a custom Instruction Set Extension (ISE) to support a dataflow based execution model. The model is a plugin of the HP-Labs [COTSon full-system simulator](#).
 - I coordinated a large group of more than ten researchers within the TERAFLUX project, by providing the core idea of a dataflow based scheduler, constant supervision and the leadership of the project.
- SW4. 2010(Jun) The ERA BENCHMARK-SUITE <http://www.dii.unisi.it/~giorgi/ebs>
- A benchmark suite for research on embedded system for mobile.

- I coordinated a large group of more than ten researchers within the ERA project, by providing the core of a public set of benchmarks for embedded applications for mobile platforms, constant supervision and the leadership of the project.
- SW3. 2004(May) The WEBMIPS: Web-based MIPS simulator <http://www.dii.unisi.it/~giorgi/WEBMIPS> and a revived version in PHP coming from the WebRISC-V project (see above) <http://www.dii.unisi.it/~giorgi/WebMIPS>
- Simulates a MIPS pipeline inside a web browser. The architectural elements are visualized while instructions pass through the pipeline.
 - This started as a student project and I supervised the realization of this tool which led to a highly cited publication.
 - The WebMIPS is a PHP edition of WEBMIPS (originally written in ASP), realized as part of a Bachelor thesis.
- SW2. 2003(Sep) The BASICRYPT BENCHMARK-SUITE <http://www.dii.unisi.it/~giorgi/basicrypt>
- A benchmark suite for research on Elliptic Curve Cryptography.
 - I coordinated a group of researchers within a FIRB project, by providing the core of a public set of benchmarks for cryptography based on Elliptic Curves.
- SW1. 2003(June) JCACHESIM cache+CPU web-based simulator <http://www.dii.unisi.it/~giorgi/jcachesim>
- Simulates a cache memory and its internal operation, while executing simple MIPS programs. It runs in a java enabled web browser.
 - This project originated from a Master thesis that I supervised and migrated from an old MS-DOS interface the full capabilities to a Java applet, while adding the cross-compilation of MIPS code.

16 Public Talks

- T47. 2019(Sep), (Italian Workshop on High Performance Computing, University of Bologna, Italy), “Data-Flow based HPC” (presentation)
- T46. 2019(Jul), (High Performance Computing and Simulation Conference, Dublin, IE), “Bridging a Data-Flow Execution Model to a Simple Programming Model” (presentation)
- T45. 2019(Jul), (Department of COmputer Science, University of Pisa, Italy), “DataFlow-Threads (DF-Threads): An Execution Model for Scalable Systems ” (presentation)
- T44. 2019(Jun), (Workshop on Computer Architecture Education (WCAE-2019)), “WebRISC-V: a Web-Based Education-Oriented RISC-V Pipeline Simulation Environmen” (presentation)
- T43. 2019(Mar), (Conference on Design, Automation and Test in Europe (DATE-2019)), “AXIOM: A Scalable, Efficient and Reconfigurable Embedded Platform” (presentation)
- T42. 2019(Feb), (IEEE Euromicro Int.l Conf. on Parallel, Distributed, and Network-Based Processing), “Analyzing the Impact of Operating System Activity of different Linux Distributions in a Distributed Environment” (presentation)
- T41. 2019(Jan), (11th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools), “A Design Space Exploration Tool Set for Future 1K-core High-Performance Computers” (presentation)
- T40. 2018(Sep), (Third Italian Workshop on Embedded Systems), “The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board” (presentation)
- T39. 2018(Jan), (SHiP-CPS: Software-Hardware Platforms for Cyber-Physical Systems), “The AXIOM platform for Cyber-Physical Systems” (presentation)
- T38. 2017(Sep), (Second Italian Workshop on Embedded Systems), “The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board” (presentation)
- T37. 2018(Jun), (Keynote Speech at IEEE MECO conference), “The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board” (presentation)
- T36. 2016(Sep), (First Italian Workshop on Embedded Systems), “AXIOM: A 64-bit scalable embedded system including Arduino socket and on-chip FPGA” (presentation)
- T35. 2016(Sep), (VIMAR, Marostica, Italy), “AXIOM Operating System analysis” (presentation)
- T34. 2016(Jun), (Barcelona Supercomputing Center, Barcelona, Spain), “AXIOM Design Exploration Tools” (presentation)
- T33. 2016(Apr), (ARTEMIS Spring Event, Vienna, Austria), “The AXIOM Cyber Physical System” (presentation)
- T32. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), “The AXIOM project” (presentation)
- T31. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), “The COTSon simulation environment” (tutorial)
- T30. 2015(Feb), (CEA conference, Dubai, UAE), “Accelerating Haskell on a Dataflow Architecture: a case study including Transactional Memory”

- T29. 2014(Oct), (MPP Workshop, Paris, France), “An Introduction to DF-Threads and their Execution Model”
- T28. 2014(Sep), (Istituto di Calcolo ad Alte Prestazioni, Napoli, Italy), “TERAFLUX: Harnessing 1 TERA devices in a single package”
- T27. 2013(Aug), (Georgia Tech, Atlanta, GA, USA), “TERAFLUX overview and the T* instruction extension”
- T26. 2013(Aug), (University of Delaware, DE, USA), “TERAFLUX Research Overview”
- T25. 2013(Oct), (SoC conference, Tampere, FI), “The TERAFLUX Project OVERVIEW” (presentation)
- T24. 2013(Oct), (SoC conference, Tampere, FI), “MANY-CORE CHIPS and New High-Performance Computing Platforms: Hardware Thread-Level Parallelism Support in Many-Core Architectures” (tutorial)
- T23. 2013(Jun), (CASTNESS workshop, Barcelona, Spain), “The T* Instruction Set Extension” (presentation)
- T22. 2013(May), (University of Pisa, Italy), “DATAFLOW: different answer to achieve Scalability” (tutorial)
- T21. 2013(Mar), (DATE Conference, Grenoble, France), “Lessons learned from European Projects” (Panel)
- T20. 2013(Feb), (University of Siena, Italy), “Creation and Management a Large Scale search Project”
- T19. 2012(Jun), (), “TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices”
- T18. 2012(May), (Computing Frontiers conference, Cagliari, Italy), “TERAFLUX: Exploiting Dataflow Parallelism Teradevice Computing”
- T17. 2012(Jun), (CASTNESS workshop, Paris, France), “TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices”
- T16. 2011(Oct), (DFM Workshop, Galveston, TX, USA), “Data Flow Execution models” (panelist)
- T15. 2011(Apr), (ODES workshop, CGO Conference, Chamonix, France), “TERAFLUX: exploiting DATAFLOW parallelism” (Keynote speech)
- T14. 2011(Jan), (CASTNESS workshop, Rome, Italy), “Overview of a TERAFLUX-like Architecture”
- T13. 2010(Jun), (International Forum on Multicores), “Integrating multicore research and the COTSon simulation platform”
- T12. 2010(May), (HiPEAC Computing Week, Edinburgh UK), “TERAFLUX: exploiting DATAFLOW parallelism”
- T11. 2005(May), (Dept. of Electronics and Information Systems, Ghent, Belgium), “Tiled Architectures for Embedded Systems”
- T10. 2004(Oct), (Dept. of Computer Engineering, Delft, Olanda), “Non- Conventional Microprocessor Architectures”
- T9. 2004(Sep), (HiPEAC Workshop, Juan les Pins, France), “Embedded-System Research Overview”
- T8. 2003(Nov), (University of Pisa, Italy), “Non-Conventional Microprocessor Architectures”
- T7. 2002(Jan), (SSGRRw-2002 Conference, L’Aquila, Italy), “Non-Conventional Microprocessor Architectures”
- T6. 2001(Nov), (SGS-Thomson Advanced Research Laboratory, Milan, Italy), “Architetture Non-Convenzionali per Microprocessore”
- T5. 2000(Apr), (University of Siena, Italy), “Introduzione alla Architettura Scheduled Data-Flow -SDF”
- T4. 1999(May), (Dept. of Electrical and Computer Engineering, University of Alabama in Huntsville, AL, USA), “Scheduled Dataflow Architecture: problems and issues”
- T3. 1998(May), (University of Belgrade, Serbia, Yugoslavia), “Simulating Composite Workloads on Shared-Bus Symmetric Multiprocessors”
- T2. 1997(Sep), (Facoltà di Ingegneria, Università di Salerno, Benevento), “Trace Factory: a Hybrid Approach to Trace Generation for Performance Evaluation of Shared Bus Multiprocessors”
- T1. 1997(Aug), (Computer Science and Engineering Dept., University of Texas at Arlington, TX, USA), “Trace Driven Simulation of Shared-Bus Multiprocessors”

17 Supervised Collaborators/Students

1. Visiting Professor
 - 2012(Sep)-2014(May) Bruce Jacob (University of Maryland)
2. Researchers
 - 2012(Apr)-2014(Jan) Alberto Scionti
 - 2012(Apr)-2013(Apr) Marco Solinas
3. Postdocs
 - 2010(Jun)-2013(Jul) Antonio Portero

- 2012(Mar)-2013(Oct) Stamatis Kavvadias
- 2010(Jun)-2012(Jan) Yu Zhibin
- 2011(Sep)-2011(Dec) Sylvain Collange
- 2010(Jun)-2011(May) Rania Mameesh
- 2010(Jan)-2011(Jan) Vincenzo Di Massa
- 2010(Jan)-2011(Jan) Nikola Puzovic
- 2010(Apr)-2010(Jun) Andrea Casaccino
- 2007(Oct)-2008(Nov) Paolo Bennati

4. Ph.D. Students

- 2018(Nov)-present Tutoring of Ph.D. student Amin Sahebi, ciclo XXXIV.
- 2017(Oct)-present Tutoring of Ph.D. student Farnam Khalili Maybodi, ciclo XXXIII.
- 2016(Oct)-present Tutoring of Ph.D. student Marco Procaccini, ciclo XXXII.
- 2013(Nov)-2017(Jul) Tutoring of Ph.D. student Somnath Mazumdar, ciclo XXIX - Thesis title: “An Efficient NoC-based Framework to Improve Dataflow Thread Management at Runtime”
- 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Nikola Puzovic, ciclo XXI - Thesis title: “Implementing fine/medium grained TLP support in multi-core architectures”
- 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Zdravko Popovic, ciclo XXI - Thesis title: “Multithreaded Dataflow in Tiled Architectures”
- 2004(Nov)-2007(Sep) Tutoring of Ph.D. student Paolo Bennati, ciclo XX - Thesis title: “Embedded Systems: Low-Power techniques and applications”
- 2001(Nov)-2005(Apr) Co-Tutoring of Ph.D. Student Irina Branovic - Thesis title: “Architectural Support for Elliptic Curve Cryptography (ECC)”

5. Graduate Students

- 2017(Sep)-2017(Oct) Tutoring of student Farnam Khalili Maybodi
- 2016(Dec)-2017(Feb) Hosting of Ph.D. student Arthur Lorenzon, from UFRGS, Brazil - sponsored by a 3-month HiPEAC (H2020) mobility grant.
- 2014(Nov)-2015(Oct) Tutoring of Ph.D. student Nitin Satpute, ciclo XXX.
- 2012(Jan)-2014(Nov) Tutoring of Ph.D. student Cai Kang, ciclo XXVII.
- 2014(Aug)-2014(Nov) Tutoring of student Amit Fuchs
- 2013(Jul)-2014(Mar) Tutoring of student Haileyesus Kifle
- 2013(Nov)-2014(Mar) Tutoring of student Daniele Colobraro
- 2013(Apr)-2014(Jan) Tutoring of student Bogdan Azaric
- 2012(Jun)-2012(Nov) Tutoring of student Eliana Sala Mariet
- 2012(Jun)-2013(Aug) Tutoring of student Andrea Mondelli
- 2012(Jan)-2013(Apr) Tutoring of student Ho Nam
- 2010(Jul)-2011(Jan) Tutoring of student Caroline Concatto
- 2008(Sep)-2009(Jun) Tutoring of student Andrea Righi
- 2008(Feb)-2008(Sep) Tutoring of student Nenad Korolija
- 2008(Feb)-2008(Sep) Tutoring of student Roberto D’Aprile
- 2004(Sep)-2005(Oct) Tutoring of student Zdravko Popovic
- Orientation Activity for potential students coming from High School.
- Tutor for several Master Thesis, Faculty of Engineering, University of Siena.

6. Master Students

- 2019 Gianfranco Mariotti (Bachelor), “Un Ambiente di Simulazione Accessibile via Web per lo Studio della Pipeline del Processore RISC-V”.
- 2015 Ettore Chimenti (Bachelor), “Porting di un sistema operativo GNU/Linux su Single-board computer ARM”.
- 2007 Giovanni Burrelli (Bachelor), “Valutazione delle prestazioni di IBM Cell Processor nelle simulazioni finanziarie”.
- 2005 Fabio Antonio Cassini (Master), “Realizzazione del modulo aggiuntivo per un concentratore seriale su interfacce I^2C BUS e 1-wire bus”.

- 2005 Gian Lorenzo Meocci (Bachelor), “Studio e implementazione di un sistema embedded adibito al controllo del traffico”.
- 2004 Mauro Marchetti (Master), “Realizzazione di un sistema di supporto alle decisioni per investimenti in borsa basato su analisi tecnica e analisi delle notizie”.
- 2004 Christos Ververidis (Master), “Analisi delle prestazioni di sistemi di elaborazione con cache: uno strumento visuale”.
- 2001 Lorenzo Menconi (Master), “Progettazione di un sistema di supporto alle decisioni per l’investimento finanziario” (co-advisor).

18 Professional Activities

1. Founded initiatives

- 2017 Founding member of the [IEEE Special Technical Community “Parallel Model & System: Dataflow and beyond”](#)

2. Project Evaluator

- Independent Expert of the MIUR under the REPRISE database for evaluation of Fundamental Research and Industrial Research, June 2018.
- Independent Expert of the European Commission for the evaluation of CHIST-ERA (Future and Emerging Technology) 2012 - FP7 (7th Framework Programme) March 2012.
- Independent Expert of the European Commission for the evaluation of Call FET (Future and Emerging Technology) 2008 - FP7 (7th Framework Programme) Massive ICT. FP6 IST-FET-26825 SHAPES (Scalable Software Hardware Architecture Platform for Embedded Systems), November 2006 through January 2010.
- Reviewer of NWO Projects (Netherlands Research Organization) and EU projects.
- Consultant for the EU Call Objective ICT-2009.8.1: FET proactive 1: Concurrent Tera-device Computing, Brussels, Nov. 2008.
- IEEE Judge (among the 8 coming from the Industry and the Academy) for IEEE Computer Science International Design Competition (CSIDC) 2001 (<http://computer.org/csdc>) sponsored by Intel, Toshiba, Ericsson, AMD, Microsoft, Lucent, EMC, Hewlett-Packard, Sun, Motorola, to assign prizes for 70’000 USD. June-July 2001.

3. Member of Ph.D. Graduation Committees

- PhD Committee (2 candidates):[Università degli Studi di Padova, Italy](#), Milan, Italy, October 2019.
- PhD Committee (4 candidates):[Politecnico di Milano](#), Milan, Italy, February 2019.
- PhD External Evaluator:[Istituto Nazionale di Fisica Nucleare](#), Rome, Italy, December 2017.
- PhD External Evaluator:[Universitat Politècnica de València](#), Valencia, Spain, December 2016.
- PhD Committee:[Universitat Politècnica de València](#), Valencia, Spain, December 2014.
- PhD Committee:[Universitat Politècnica de Catalunya](#), Barcelona, Spain, May 2014.
- PhD Committee:[Universitat Politècnica de Catalunya](#), Barcelona, Spain, September 2011.
- PhD Committee:[Chalmers University](#), Goteborg, Sweeden, June 2011.
- PhD Committee:[Universitat Politècnica de Catalunya](#), Barcelona, Spain, December 2009.
- PhD Committee:[IMT - Institute for Advanced Studies](#), Lucca, Italy, July 2009.

4. Member of Ph.D. Selection Committees

- University of Florence, University of Pisa, University of Siena, “Smart Computing”, Sept. 2015.
- University of Siena, Dept. of Information Engineering, Sept. 2010.
- University of Siena, Dept. of Information Engineering, Sept. 2008.

5. Journal Editorial Boards

- 2017(Mar)-present Associate Editor of the [International Journal of Embedded Systems \(IJES\)](#).
- 2014(Jan)-present Member of the editorial board of the [International Journal of Embedded Systems \(IJES\)](#).
- Co-Guest Editor of ACM Computer Architecture News (official Newsletter of ACM Special Interest Group on Computer Architecture), number of December 2001, with emphasis on Compilation Techniques, Parallel Architectures and Frontiers Topics.
- Guest Editor of IEEE-TCCA NEWSLETTER (official Newsletter of IEEE Special Interest Group in Computer Architecture), number of January 2001, with emphasis on MEMory DEcoupled Architectures in modern microprocessors.

- Co-Guest Editor of Journal of Embedded Computing, 2006 special issue on Embedded Single-Chip Multicore Architectures and related research - from System Design to Application Support.
- Journal Reviewer: IEEE Transaction on Computers, IEEE Transaction on Parallel and Distributed Systems, IEEE Micro, IEEE Concurrency, Computer Journal, Journal of System Architecture, IEEE Transaction on Circuits and Systems, Elsevier Microprocessor and Microsystems, ACM Transactions on Architecture and Code Optimization (TACO), Concurrency and Computation: Practice and Experience, Elsevier Parallel Computing, Journal of Parallel and Distributed Systems.

6. Keynote Speaker

- **Keynote Speaker:** [IEEE MECO Conference 2017](#), Bar, Montenegro, June 2017.
- **Keynote Speaker:** SSGRR 2002w International Conference, L'Aquila, Italy, January 2002.

7. Chairing

- **Program Chair:** [3rd Italian Workshop on Embedded Systems](#), Siena, Italy, September 2018.
- **Program Chair:** [Software/Hardware platforms for Cyber-Physical Systems Workshop](#), Manchester, UK, January 2018.
- **General Chair:** [ACM Computing Frontiers 2017](#), Siena, Italy, May 2017.
- **Program Chair** of the European-Project track: [DATE 2016](#), Dresden, Germany, March 2016.
- **General Chair:** [CASTNESS 2012](#), Paris, France, January 2012.
- **General Co-Chair:** [HiPEAC WRC 2011](#), Heraklion, Greece, January 2011.
- **Program Co-Chair:** [HiPEAC WRC 2010](#), Pisa, Italy, January 2010.
- **Publicity Chair:** [HiPEAC 2010](#), Pisa, Italy, January 2010.
- **Financial/Local Co-Chair:** [WAIFI-2008 Workshop](#), Siena, Italy, July 2008.
- **Program Co-Chair:** [ESA-05 Conference](#), Las Vegas, Nevada, USA, June 2005.
- **General Chair:** [MEDEA-2001 Workshop](#), Barcelona, Spain (EU), September 2001.
- **Program Chair:** [MEDEA-2000 Workshop](#), Philadelphia, Pennsylvania (USA), October 2000.
- **General Chair and Founder:** [MEDEA-2000 Workshop](#), Philadelphia, Pennsylvania (USA), October 2000.

8. Program Committee Membership

- PC131. [Applied Reconfigurable Computing, ARC 2020](#), Rennes, France, June 2021.
- PC130. [IEEE MECO CPS & IoT](#), Budva, Montenegro, June 2021.
- PC129. [HiPEAC RAPIDO 2021](#), Budapest, HU, January 2021.
- PC128. [IEEE BIGDATASE-2020](#), Guangzhou, China, November 2020.
- PC127. [Field Programmable Logic Conference, FPL-2020](#), Goteborg, SW, September 2020.
- PC126. [ICPP Embedded Multicore Systems, EMS 2020](#), Edmonton, Canada, August 2020.
- PC125. [EUROMICRO DSD-2020](#), Portoroz, Slovenia, August 2020.
- PC124. [IEEE DFM-2020](#), Madrid, Spain, July 2020.
- PC123. [Workshop on Parallel Programming Models., MPP 2020](#), New Orleans, Louisiana, USA, May 2020.
- PC122. [Architecture of Computing Systems, ARCS 2020](#), Aachen, Germany, May 2020.
- PC121. [Applied Reconfigurable Computing, ARC 2020](#), Toledo, Spain, April 2020.
- PC120. [ACM SAC-2020 Special Track](#), Brno, Czech Republic, April 2020.
- PC119. [HiPEAC RAPIDO 2020](#), Bologna, IT, January 2020.
- PC118. [IEEE DFM-2019](#), Milwaukee, Wisconsin, USA, July 2019.
- PC117. [Field Programmable Logic Conference, FPL-2019](#), Barcelona, Spain, September 2019.
- PC116. [EUROMICRO DSD-2019](#), Kallithea, Chalkidiki, Greece, August 2019.
- PC115. [ICPP Embedded Multicore Systems, EMS 2019](#), Kioto, Japan, August 2019.
- PC114. [The 8th International Workshop on Advances in Parallel Programming Models and Frameworks for the Multi-/Many-core Era](#), Dublin, Ireland, July, 2019.
- PC113. [IEEE MECO-2019](#), Budva, Montenegro, June 2019.
- PC112. [Architecture of Computing Systems, ARCS 2019](#), Copenhagen, Denmark, May 2019.
- PC111. [Applied Reconfigurable Computing, ARC 2019](#), Darmstadt, Germany, April 2019.
- PC110. [HiPEAC RAPIDO 2019](#), Valencia, ES, January 2019.
- PC109. [ACM SAC-2019 Special Track](#), Limassol, Cyprus, April 2019.
- PC108. [The 18th IEEE International Conference on Scalable Computing and Communications, ScalCom-2018](#), Guangzhou, China, October 2018.
- PC107. [IEEE ReConFig 2018](#), Cancun, Mexico, December 2018.
- PC106. [Field Programmable Logic Conference, FPL-2018](#), Dublin, Ireland, August 2018.
- PC105. [ICPP Embedded Multicore Systems, EMS 2018](#), Eugene, Oregon, USA, August 2018.
- PC104. [EUROMICRO DSD-2018](#), Prague, Czech Republic, August 2018.
- PC103. [IEEE MECO-2018](#), Budva, Montenegro, June 2018.
- PC102. [Applied Reconfigurable Computing, ARC 2018](#), Santorini, May 2018.
- PC101. [ACM SAC-2018 Special Track](#), Pau, France, April 2018.

- PC100. [Architecture of Computing Systems, ARCS 2018](#), Braunschweig, Germany, April 2018.
- PC99. [HiPEAC RAPIDO 2018](#), Manchester, UK, January 2018.
- PC98. [HiPEAC WRC WRC 2018](#), Manchester, UK, January 2018.
- PC97. [IEEE ReConFig 2017](#), Cancun, Mexico, December 2017.
- PC96. [SBACPAD-2017](#), Campinas, Brazil, October 2017.
- PC95. [IEEE FPL-2017](#), Ghent, Belgium, September 2017.
- PC94. [ICPP Embedded Multicore Systems, EMS 2017](#), Bristol, UK, August 2017.
- PC93. [IEEE MSPDS 2017](#), Genova, Italy, July 2017.
- PC92. [IEEE MECO-2017](#), Bar, Montenegro, June 2017.
- PC91. [ACM SAC-2017 Special Track](#), Marrakesh, Morocco, April 2017.
- PC90. [Applied Reconfigurable Computing, ARC 2017](#), Delft, Netherlands, April 2017.
- PC89. [Architecture of Computing Systems, ARCS 2017](#), Vienna, Austria, April 2017.
- PC88. [HiPEAC Embedded 2017](#), Nurnberg, February 2017.
- PC87. [HiPEAC RAPIDO 2017](#), Stockholm, Sweden, January 2017.
- PC86. [HiPEAC WRC WRC 2017](#), Stockholm, Sweden, January 2017.
- PC85. [ICPP Embedded Multicore Systems, EMS 2016](#), Philadelphia, PA, USA, August 2016.
- PC84. [IEEE ReConFig 2016](#), Cancun, Mexico, November 2016.
- PC83. [IEEE DFM-2016](#), Haifa, Israel, September 2016.
- PC82. [IEEE FPL-2016](#), Lausanne, Switzerland, August 2016.
- PC81. [IEEE MECO-2016](#), Bar, Montenegro, June 2017.
- PC80. [ACM SAC-2016 Special Track](#), Pisa, Italy, April 2016
- PC79. [IEEE MSPDS 2016](#), Innsbruck, Austria, July 2016.
- PC78. [Architecture of Computing Systems, ARCS 2016](#), Nurnberg, April, 2016.
- PC77. [HiPEAC WRC 2016](#), Prague, Czech Republic, January 2016.
- PC76. [HiPEAC RAPIDO 2016](#), Prague, Czech Republic, January 2016.
- PC75. [IEEE DFM-2015](#), San Francisco, CA, USA, October 2015.
- PC74. [IEEE ICCD-2015](#), New York, USA, October 2015.
- PC73. [IEEE FPL-2015](#), London, UK, September 2015.
- PC72. [IEEE WCS-IOT 2015](#), London, UK, September 2015.
- PC71. [EUROMICRO DSD-2015](#), Funchal, Madeira, Portugal, August 2015.
- PC70. [IEEE M2A2-2015](#), New York, USA, August 2015.
- PC69. [WRC-2015 Workshop](#), Amsterdam, Netherlands, January 2015.
- PC68. [MULTIPROG-2015 Workshop](#), Amsterdam, Netherlands, January 2015.
- PC67. [ARCS-2015](#), Porto, Portugal, March 2015.
- PC66. [ACM SAC-2015 Special Track](#), Salamanca, Spain, April 2015.
- PC65. [IEEE ICPADS-2014](#), Hsinchu, Taiwan, December 2014.
- PC64. [IEEE ICCD-2014](#), Seoul, Korea, October 2014.
- PC63. [IEEE FPL-2014](#), Munich, Germany, September 2014.
- PC62. [IEEE DFM-2014](#), Edmonton (Alberta), Canada, August 2014.
- PC61. [IEEE M2A2-2014](#), Paris, France, August 2014.
- PC60. [2014 ACM International Conference on Supercomputing \(ICS\)](#), (External Review Committee), Munich, Germany, June 2014.
- PC59. [ACM SAC-2014 Special Track](#), Gyeongju, South Korea, March 2014.
- PC58. [ARCS-2014](#), Lubeck, Germany, February 2014.
- PC57. [MULTIPROG-2014 Workshop](#), Vienna, Austria, January 2014.
- PC56. [IEEE ICPADS-2013](#), Seoul, Korea, December 2013.
- PC55. [IEEE ICCD-2013](#), Asheville, NC, USA, October 2013.
- PC54. [IEEE DFM-2013](#), Edinburgh, UK, September 2013.
- PC53. [IEEE FPL-2013](#), Porto, Portugal, August 2013.
- PC52. [IEEE M2A2-2013](#), Melbourne, Australia, July 2013.
- PC51. [HiPEAC WRC 2013](#), Berlin, Germany, January 2013.
- PC50. [ACM SAC-2013 Special Track](#), Trento, Italy, March 2013.
- PC49. [ARCS-2013](#), Prague, Czech Republic, February 2013.
- PC48. [MULTIPROG-2013 Workshop](#), Berlin, Germany, January 2013.
- PC47. [IEEE FPL-2012](#), Oslo, Norway, August 2012.
- PC46. [IEEE M2A2-2012 Workshop](#) IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms, Madrid, Spain, July 2012.
- PC45. [IEEE ICCD-2012](#), Montreal, Quebec, Canada, September 2012.
- PC44. [Workshop on the Growing Problems with Scalable Heterogeneous Infrastructures \(GSHI'12\)](#), Madrid, Spain, July 2012.
- PC43. [HiPEAC WRC 2012](#), Paris, France, January 2012.
- PC42. [ACM SAC-2012 Special Track](#), Trento, Italy, March 2012.
- PC41. [ARCS-2012](#), Munich, Germany, February 2012.
- PC40. [MULTIPROG-2012 Workshop](#), Paris, France, January 2012.
- PC39. [IEEE SEC-2011](#), Sydney, Australia, December 2011.
- PC38. [IEEE ICCD-2011](#), Amherst, MA, USA, October 2011.
- PC37. [IEEE FPL-2011](#), Chania, Greece, September 2011.
- PC36. [ACM SAC-2011 Special Track](#), TaiChung, Taiwan, March 2011.

- PC35. [ARCS-2011](#), Lake Como, Italy, February 2011.
- PC34. [MULTIPROG-2011 Workshop](#), Heraklion, Greece, January 2011.
- PC33. [IEEE ICCD-2010](#), Amsterdam, Netherlands, October 2010.
- PC32. [IEEE FPL-2010](#), Milano, Italy, August 2010.
- PC31. [MULTIPROG-2010 Workshop](#), Pisa, Italy, January 2010.
- PC30. [ACM SAC-2010 Special Track](#), Sierre, Switzerland, March 2010.
- PC29. [IEEE ICCD-2009](#), Lake Tahoe, California (USA), October 2009.
- PC28. [WoRMES 2009](#), Vancouver, Canada, August 2009.
- PC27. [ICPP 2009](#), Vienna, Austria, September 2009.
- PC26. [Computing Frontiers 2009](#), Ischia, Italy, May 2009.
- PC25. [ACM SAC-2009 Special Track](#), Honolulu, Hawaii (USA), March 2009.
- PC24. [MULTIPROG-2009 Workshop](#), Paphos, Cyprus, January 2009.
- PC23. [IEEE ICCD-2008](#), Lake Tahoe, California (USA), October 2008.
- PC22. [MEDEA-2008 Workshop](#), Toronto, Canada, October 2008.
- PC21. [IEEE SEC-2008](#), Beijing, China, October 2008.
- PC20. [MEDEA-2008 Workshop](#), Toronto, Canada, October 2008.
- PC19. [IEEE SEC-2008](#), Beijing, China, October 2008.
- PC18. [ACM SAC-2008 Special Track](#), Fortaleza, Brazil, March 2008.
- PC17. [MULTIPROG-2008 Workshop](#), Goteborg, Sweden, January 2008.
- PC16. [MEDEA-2007 Workshop](#), Brasov, Romania, September 2007.
- PC15. [HiPEAC 2007 Conference](#), Ghent, Belgium, January 2007.
- PC14. [ACM SAC-2007 Special Track](#), Seoul, Korea, March 2007.
- PC13. [MEDEA-2006 Workshop](#), Seattle, Washington, USA, September 2006.
- PC12. [ACM SAC-2006 Special Track](#), Dijon, France, April 2006.
- PC11. [HiPEAC 2005 Conference](#), Barcelona, Spain, November 2005.
- PC10. [MEDEA-2005 Workshop](#), Saint Louis, Missouri, USA, September 2005.
- PC9. [SCOPES-2005 Workshop](#), Dallas, Texas, USA, September 2005.
- PC8. [PDES-05 IEEE/IFIP Workshop](#), Fukuoka, Japan, July 2005.
- PC7. [ACM SAC-2005 Special Track](#), Santa Fe, New Mexico, USA, March 2005.
- PC6. [MEDEA-2004 Workshop](#), Antibes Juan-les-Pins, France, September 2004.
- PC5. [ACM SAC-2004 Special Track](#), Nicosia, CIPRO, March 2004.
- PC4. [MEDEA-2003 Workshop](#), New Orleans, Louisiana (USA), September 2003.
- PC3. [ACM SAC-2003 Special Track](#), Melbourne, Florida (USA), March 2003.
- PC2. [PACT-2002 Conference](#), Charlottesville, Virginia (USA), September 2002.
- PC1. [MEDEA-2002 Workshop](#), Charlottesville, Virginia (USA), September 2002.

19 Major Departmental Committees

- 2006 **President** of the Self-Evaluation Committee (RAV) for the Information Engineering Laurea.
- 2018(Oct)-present **Scientific Director of the University of Siena** in the Italian Academic Consortium for Informatics (CINI).
- 2018(Oct)-present **Delegate of the University of Siena (appointed by the Ministry)** in the Italian Academic Consortium for Informatics (CINI).
- 2018(Mar)-present **Department Deputy** for the University of Siena Alumni Association.
- 2015(Jun)-present **Member of Ph.D. Committee “Smart Computing”** (Uni. of Florence, Pisa, Siena).
- 2014-present Member of the Student Tutoring Committee for the University of Siena.
- 2019-present Member of the Orientation commission.
- 2010-present Member of Admission Committee to the Master Degrees.
- 2000-present President and member of several selection procedure for Ph.D. grants (2 times), Postdoc grants (5+ times), Post-laurea grants (5+ times).
- 2012(Nov) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2012-2015 Member of Department Committee for the Management of Scientific spaces.
- 2002-2010 Member of Ph.D. Committee (Department of Information Engineering, Siena).
- 2001-2010 Member of Local Area Network Management (Department Information Engineering, Siena).
- 2006-2009 Member of the Evaluation Board for Master and Bachelor Degree in Computer Engineering (Faculty of Engineering, Siena).

- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2001-2009 Member of the Evaluation Board for Master in New Technologies and Company Management (University of Siena).
- 2005(Oct) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2000-2005 Member of the Orientation and Tutoring commission.
- 2000-2005 Design and Maintenance of Orientation WEB Site, Faculty Engineering, Siena (www.ing.unisi.it/orientamento - www.ing.unisi.it/orientamento/initinere - www.ing.unisi.it/orientaing).

(continues)

20 Teaching

The following courses have been taught at the University of Siena at the School of Engineering, at the School of Economics and at the S.Chiana College. From year 2000 until now, more than 365 ECTS credits¹ have been taught (corresponding to an average of about 18 credits per year).

As Associate Professor:

Year	Course	ECTS credits	Level	School	Lang.
2019-2020	Advanced Computer Architecture	9	Master	Information Engineering	English
2019-2020	Computer Architecture	6	Bachelor	Information Engineering	Italian
2018-2019	Advanced Computer Architecture	9	Master	Information Engineering	English
2018-2019	Computer Architecture	6	Bachelor	Information Engineering	Italian
2017-2018	Advanced Computer Architecture	9	Master	Information Engineering	English
2017-2018	Computer Architecture	6	Bachelor	Information Engineering	Italian
2016-2017	Advanced Computer Architecture	9	Master	Information Engineering	English
2016-2017	Computer Architecture	6	Bachelor	Information Engineering	Italian
2015-2016	Advanced Computer Architecture	9	Master	Information Engineering	English
2015-2016	Computer Architecture	6	Bachelor	Information Engineering	Italian
2014-2015	Advanced Computer Architecture	9	Master	Information Engineering	English
2013-2014	Advanced Computer Architecture	9	Master	Information Engineering	English
2013-2014	Computer Architecture	6	Bachelor	Information Engineering	Italian
2012-2013	Advanced Computer Architecture	9	Master	Information Engineering	English
2012-2013	Computer Architecture	6	Bachelor	Information Engineering	Italian
2011-2012	Advanced Computer Architecture	9	Master	Information Engineering	Italian
2011-2012	Computer Architecture	6	Bachelor	Information Engineering	Italian
2010-2011	Advanced Computer Architecture	9	Master	Information Engineering	Italian
2010-2011	Computer Architecture	6	Bachelor	Information Engineering	Italian
2009-2010	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2009-2010	Computer Architecture	6	Bachelor	Information Engineering	Italian
2008-2009	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2008-2009	Computer Architecture	6	Bachelor	Information Engineering	Italian
2007-2008	Low Power Architectures	2	Ph.D.	Information Engineering	Italian
2007-2008	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2007-2008	Information Security	3	Master	Management of Financial Inst.	Italian
2007-2008	Computer Architecture	6	Bachelor	Information Engineering	Italian
2006-2007	Low Power Architectures	2	Ph.D.	Information Engineering	Italian
2006-2007	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2006-2007	Information Security	3	Master	Management of Financial Inst.	Italian
2006-2007	Computer Architecture	6	Bachelor	Information Engineering	Italian
2005-2006	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2005-2006	Information Security	3	Master	Management of Financial Inst.	Italian
2005-2006	Computer Architecture	6	Bachelor	Information Engineering	Italian

As Assistant Professor:

Year	Course	ECTS credits	Level	School	Lang.
2004-2005	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2004-2005	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2004-2005	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2003-2004	C++ Programming Laboratory	2	Master	Information Engineering	Italian
2003-2004	Programming Fundamentals	3	Master	Digital Economy and E-business	Italian
2003-2004	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2003-2004	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2002-2003	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2002-2003	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2002-2003	Programming Fundamentals	3	Master	Digital Economy and E-business	Italian
2002-2003	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2002-2003	Computer Architecture	6	Bachelor	Information Engineering	Italian
2002-2003	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2001-2002	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2001-2002	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2001-2002	Computer Architecture	6	Bachelor	Information Engineering	Italian
2001-2002	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Database management	3	Bachelor	Management of Financial Inst.	Italian
2000-2001	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2000-2001	Database management	3	Master	Management of Financial Inst.	Italian
2000-2001	Computer Architecture	6	Bachelor	Information Engineering	Italian
1999-2000	Advanced Computer Architecture	12	Master	Information Engineering	Italian
1999-2000	Computer Architecture	6	Bachelor	Information Engineering	Italian

International Teaching

¹One ECTS credit corresponds to about 10 hours of teaching and 15 additional hours of personal study of the student.

Prof. Giorgi held invited lectures on "Multi-Core and Many-Core architectures" at the University of Tampere, Finland in October 2013.

21 Coordination of Teaching and Research Activities

- 2014-present **co-founder** of the "[CompuThink Lab](#)" as a representative of the "Computer Architecture Lab".
- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2007-present **co-responsible** of the "Computer Architecture Lab", with more than 30 workstations, major computing facilities and having equipment and donations from "AMD", "HP-Labs", "Intel", "NVIDIA", "SECO", "ST-Microelectronics", "Xilinx".

22 Citations by Patents

According to IEEEExplore, Roberto Giorgi's papers have been cited by the following patents:

1. Dubrulle, Paul; Goubier, Thierry, and Stéphane Louise, "Speculative and iterative execution of delayed data flow graphs." U.S. Patent Application 10/394,729, filed August 27, 2019.
2. Manet, Philippe; Rousseau, Bertrand, "Tile-based processor architecture model for high-efficiency embedded homogeneous multicore platforms", Patent No. 9275002
3. Manet, Philippe; Rousseau, Bertrand, "A TILE-BASED PROCESSOR ARCHITECTURE MODEL FOR HIGH EFFICIENCY EMBEDDED HOMOGENEOUS MULTICORE PLATFORMS", Patent No. EP2531929
4. Manet, Philippe; Rousseau, Bertrand, "A TILE-BASED PROCESSOR ARCHITECTURE MODEL FOR HIGH EFFICIENCY EMBEDDED HOMOGENEOUS MULTICORE PLATFORMS", Patent No. WO2011092323
5. Rowlands, Joseph B., "BRIDGES PERFORMING REMOTE READS AND WRITES AS UNCACHEABLE COHERENT OPERATIONS", Patent No. 7752281
6. Sano, Barton J.; Rowlands, Joseph B.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS USING MIX OF PACKET COHERENT AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS", Patent No. 7424561
7. Sano, Barton J., "SYSTEM HAVING CONFIGURABLE INTERFACES FOR FLEXIBLE SYSTEM CONFIGURATIONS", Patent No. 7394823
8. Rowlands, Joseph B., "SYSTEM HAVING INTERFACES SWITCH AND MEMORY BRIDGE FOR CC NUMA OPERATION", Patent No. 7266587
9. Sano, Barton J.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS INCLUDING PACKET INTERFACES SWITCHES AND PACKET DMA CIRCUITS FOR SPLITTING AND MERGING PACKET STREAMS", Patent No. 7227870
10. Sano, Barton J.; Rowlands, Joseph B.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS USING MIX OF PACKET COHERENT AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS", Patent No. 7206879
11. Rowlands, Joseph B., "SYSTEM HAVING ADDRESS BASED INTRANODE COHERENCY AND DATA BASED INTERNODE COHERENCY", Patent No. 7003631
12. Rowlands, Joseph B., "L2 CACHE MAINTAINING LOCAL OWNERSHIP OF REMOTE COHERENCY BLOCKS", Patent No. 6993631
13. Rowlands, Joseph B.; Keller, James B., "REMOTE LINE DIRECTORY WHICH COVERS SUBSET OF SHAREABLE CC NUMA MEMORY SPACE", Patent No. 6965973
14. Sano, Barton J.; Rowlands, Joseph B.; Keller, James B.; Moll, Laurent R.; Oner, Koray; Gulati, Manu, "SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC", Patent No. 6941406
15. Sano, Barton J.; Oner, Koray; Moll, Laurent R.; Gulati, Manu, "SYSTEM HAVING TWO OR MORE PACKET INTERFACES A SWITCH AND A SHARED PACKET DMA CIRCUIT", Patent No. 6912602
16. Sano, Barton J.; Rowlands, Joseph B.; Keller, James B.; Moll, Laurent R.; Oner, Koray; Gulati, Manu, "SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC", Patent No. 6748479
17. Rowlands, Joseph B., "System with address-based intranode coherency and data-based internode coherency", Patent No. EP1363191
18. Lin, Chi-Hung; Liao, Che-Yu; Chuang, Ching-Hsiang; Tung, Shing-Wu, "Hybrid simulation system and method", Patent No. 8645116

19. Attinella, John Eric, "CREATING A PHYSICAL TRACE FROM A VIRTUAL TRACE", Patent No. 7853928
20. Dageville, Benoit; Muthukrishnan, Sambavi; Zait, Mohamed, "TECHNIQUES FOR DETERMINING EFFECTS ON SYSTEM PERFORMANCE OF A MEMORY MANAGEMENT PARAMETER", Patent No. 7539608
21. Gupta, Vidyabhusan, "SYSTEM AND METHOD FOR DESIGNING AND OPTIMIZING THE MEMORY OF AN EMBEDDED PROCESSING SYSTEM", Patent No. 7412369