Dynamically Reconfiguring through Phase Detection on FPGA

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ABSTRACT

we propose a new framework based on Xilinx Virtex-6 platform for the implementation of task-optimized coarse-grained reconfiguration that can be reconfigured to adapt to the applications’ behavior. We use MicroBlaze as a general-purpose processor and a ρ-VEX VLIW architecture as reconfigurable cores. A run-time component called supervisor, dynamically monitors the system behavior, and triggers the reconfiguration; we also propose a Profiler component that automatically obtains the phase information. The collected data can be used to guide dynamic reconfiguration on the FPGA.

Proposed The Phase Detection Framework on FPGA

The general-purpose processor:
Xilinx MicroBlaze™ soft core

The reconfigurable cores:
ρ-VEX VLIW Processor

The p-profiler component is in charge of classifying phases, the supervisor dynamically monitors the application behavior, and detects the different phases to trigger the reconfiguration.

Phase Classification Based on FPGA

- **Program Structure Analyzer**
  According to the structure being used, it analyzes the structure, marking its start and the end points. It provides this information as input to the next block.

- **Program Structure Data**
  Gather input metric for phase classification.

- **Phase classification Block**
  Extracts the phases according to the selected metrics. If a phase is not present in the phase state block, assign a new ID, otherwise, the code segment is considered.

- **Phase State Block**
  Record phases and the corresponding code segment IDs.

- **Efficiency Evaluator**
  Compute power consumption and execution time, providing the needed information to support supervisor making decisions, make the system working with the optimal configuration.

- **Control block**
  Interacts among phase classification block, efficiency evaluator and supervisor.

- **Supervisor**
  Triggers the hardware reconfiguration, according to the phase state and the efficiency evaluation.

Conclusions

To help FPGA platform reconfiguring its resources dynamically, we studied the online phase classification on FPGA problem. We use the supervisor to monitor the behavior of program and based on the program phases to trigger reconfiguration. Also we take power consumption and execution time as the reference parameters to help supervisor to make the decisions, keeping a minimum reconfiguration time in order to have no effect on the

References


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